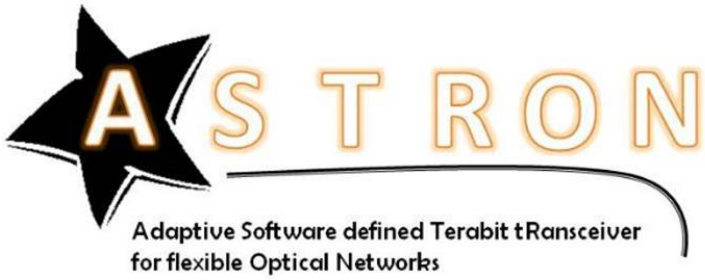

ADAPTIVE SOFTWARE DEFINED TERABIT TRANSCEIVER FOR FLEXIBLE OPTICAL NETWORKS

FP7-ICT-GA 318714

SPECIFIC TARGETED RESEARCH PROJECT (STREP)INFORMATION & COMMUNICATION TECHNOLOGIES (ICT)

Techno-economic analysis with respect to green aspects and cost

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Abstract

This deliverable reports on the benefits of introducing the ASTRON project transceiver solutions in a flexible optical network. It summarises the results of extensive studies and analysis with the purpose to: a) identify the system performance limitations, in terms of achieved flexibility and bandwidth utilisation improvement, b) calculate the expected implementation cost of the proposed OFDM adaptive software-defined transmitter and receiver modules in order to identify the economic benefits of the ASTRON project solutions, and c) evaluate the overall energy consumption of the ASTRON solutions to evaluate their environmental footprint. In all cases, comparisons are made with legacy technologies and Nyquist-WDM based solutions.

The ASTRON Project Consortium

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Executive summary

ASTRON aims at the development of high-capacity, energy-efficient and bit-rate flexible optical transceivers capable of supporting rates from 10 Gbps to beyond 1 Tbps. The ASTRON concept combines monolithic and hybrid integration to develop, for the first time, complex super-channel OFDM/Nyquist-WDM transmitters and receivers relying on an integrated arrayed waveguide grating as the key element for super-channel multiplexing/demultiplexing.

In this report, we estimate the expected implementation cost and power consumption of the proposed adaptive software-defined super-channel transmitter and receiver modules in order to identify the economic benefits, in terms of both total equipment cost and overall energy consumption (or, equivalently, annual electricity cost) of the ASTRON project solutions, namely, the filter-bank based OS-OFDM solution and the AO-OFDM (with and without DSP at the receiver). Comparisons are made with legacy single-carrier and multi-carrier solutions, in particular, Nyquist-WDM transceiver solutions based on both digital and optical Nyquist-shaping filters at the transmitter. The cost and power consumption model also addresses the node technologies. We assume conventional colourless-directionless, and colourless-contentionless flexible-grid route and select ROADM architectures for the single-carrier transmission scenarios, as well as two-tier ROADM architectures with all-optical sub-channel add-drop capability, enabling super-channel routing at the sub-channel and super-channel levels, for the super-channel transmission scenarios.

In order to take into account the uncertainty of a number of cost values in our reference model, we perform a sensitivity analysis of the super-channel transceiver cost on the cost of the optical Nyquist-shaping filters and the potential transceiver cost reductions due to integration and packaging. One result of this analysis is that the Nyquist-WDM transceivers based on optical filtering can become an interesting alternative to transceivers based on digital filtering at the DSP module if the estimated new technology cost of the Nyquist-shaping high-spectral-resolution (HSR) filter decreases by ~26% on account of technology maturity and mass production (which, assuming a similar market evolution for WSS and HSR filters, is a realistic assumption since currently commercial 1×9 WSSs are around 40% less expensive than the HSR filter, according to our estimations). It is therefore expected that the HSR filter cost could drop to that of a 1×9 WSS, in which case the optical-filter-based transceiver would be more cost-effective than those based on digital filtering. Another result is that the cost performance of the ASTRON transceiver solutions relies to a great extent on the ability to significantly lower the manufacturing costs through integration (leading to packaging savings due to the transfer of a number of connections and functions from the backend to the frontend). Current research attempts at monolithic integration of several OFDM sub-channels in a single PIC have prompted a superlinear increase in PIC size (due to hybrid assembly at a single interface, waveguide length adjustment sections for signal synchronization, etc.) and lower yields. We have observed that the size of a Tx PIC integrating 4 channels quadruples that of a 2-ch PIC, and the size of a Tx PIC integrating 8 channels septuples or even octuples that of a 2-ch PIC. Likewise, in a first approximation, the manufacturing yield of a PIC integrating N channels decreases exponentially with N and therefore the yield of an 8-ch PIC reduces to 0.2 if the single-channel PIC yield is as low as 0.9. However, advantages of monolithic integration can be envisaged in terms of performance and compactness, as well as simplification of packaging, assembly and testing, which nowadays dominate the cost of optical components. Further improvements in InP technology and process control, as well as larger wafer sizes (than the 3-4 inch wafers currently used), are expected to boost the benefits of monolithic integration.

The ASIC module represents 20%-50% of the total transceiver cost depending mainly on (a) the employed CMOS technology and (b) whether or not system vendors have in-house DSP chip development capability, but also, to a lesser extent, on (c) integration and packaging savings and (d) the number of integrated sub-channels. In ASTRON we have estimated the ASIC to account for ~49% of the total cost, and therefore a reduction in the DSP cost of, say, ~40% would result in an overall transceiver cost reduction of ~27%. It is then clear that reducing the CMOS process size is, together with monolithic integration, the single most far-reaching mechanism to reduce the transceiver cost.

Moreover, using smaller CMOS process sizes would also have a massive impact on the overall transceiver power consumption since the ASIC accounts for more than 70% of the power consumption of the transceiver. This can be further enhanced by reducing the complexity of the DSP algorithms. We report in this document that the ASTRON-project filter-bank-based OS-OFDM super-channel solution can provide around 44% total-ASIC-complexity reduction in comparison with a conventional transceiver, while ensuring a good transmission performance (note that the DSP complexity in the ASTRON-project transceiver is fundamentally due to the receiver part). Modelling studies suggest that moving from 40nm to 20nm to 16nm would reduce the power consumption by approximately 30-40% in each process step, which combined with the savings brought about by the filter-bank approach, could enable energy savings slightly in excess of 70% with 20nm and up to 75-85% with 16nm. This would make it possible for an integrated super-channel transceiver to reduce its power consumption to that of a 100G long-haul line card –including OIF MSA module based on the 40nm CMOS technology, OTU framer and client modules (~150W)–, thereby dividing by eight the environmental footprint of the ASTRON solutions in comparison with transmission scenarios relying on currently available 100G single-carrier transceivers.

The cost and power consumption reference model described in this document is used to perform a network-wide techno-economic evaluation. We consider a European backbone network (France Telecom national network) and an all-optical traffic grooming RMLSA algorithm to maximize the network-level performance of the super-channel transmission solutions. Based on it, the performance of the ASTRON solutions is compared with legacy technologies. The results of this techno-economic analysis show a linearly increasing network performance improvement for the ASTRON solutions with respect to the benchmarking multi-line-rate (MLR) scenario (relying on single-carrier transceivers capable of varying the modulation format from DP-BPSK to DP-16QAM), with spectral savings amounting to 15% when the total load reaches 226 Tb/s. For low total offered loads, MLR is the best solution because it exhibits a good network performance and is the most cost-effective solution. Conversely, the ASTRON solutions offer cost benefits for loads above 125 Tb/s, with savings of up to 30% when the load equals 226 Tb/s. An additional cost reduction of up to 25% can be achieved through further integration and packaging transceiver cost reductions. Regarding the power consumption, the ASTRON solutions outperform again the MLR scenario for loads in excess of 150 Tb/s, with energy savings amounting to 8% when the total load reaches 226 Tb/s. These savings increase to 21% and 30%, respectively, if the DSP power can be brought down to 24W (38% reduction) and 19.25W (50% reduction). In these cases, the total offered load from which the ASTRON solutions outperform the MLR scenario drops to 90 Tb/s and 65 Tb/s, respectively.

The outcome of this deliverable is meant to help network operators and potential consumers assess both direct and indirect costs and benefits related to the deployment of the ASTRON super-channel transceiver solutions.

1. Introduction

Triggered by emerging services such as high-definition video distribution, cloud computing, and social networking, the IP traffic volume has been exponentially increasing. It is expected that the global IP traffic volume surpasses the zettabyte threshold by the end of 2017 [1] and becomes extremely heterogeneous and time varying. As a consequence, network operators will require a new generation of optical transport networks in the near future to efficiently serve this colossal and heterogeneous volume of traffic in a cost-effective and scalable manner.

In response to these large capacity and disparate traffic granularity needs of the future Internet, flexible optical network architectures have been proposed [2]. Such networks rely on the capability to assign a spectrum portion, data rate and modulation format to bandwidth adaptable connections, with the aim of optimizing the use of the network resources and reducing the ecological impact of the network operation.

The ASTRON project proposes a software-defined transceiver with improved and heterogeneous transmission characteristics based on OFDM that enables the wide and cost-efficient deployment of flexible core networks. This is achieved by the design and development of cost-optimised, compact and scalable photonic integrated components as well as all the necessary electronic circuits and state of the art algorithms to drive and control the optical devices.

To study the benefits introduced by the ASTRON transceiver solutions, a cost-benefit analysis is performed in this deliverable. To do so, after the development of the cost and power consumption model for the network elements (transceivers and ROADMs), and the selection of the benchmarking scenarios, the total cost of ownership for benchmarks and ASTRON solution is calculated and a comparison between them is drawn. To provide a wider outlook the network-level studies have been carried out with both single- and multi-layer approaches, and therefore the outcome of this deliverable is a good measure for determining the total economic value of the ASTRON solutions. Due to the special significance of the DSP module in terms of power consumption (>75% of the power consumption of a 100G transceiver is DSP-related), a complexity and power consumption analysis has also been carried out for different linear and nonlinear equalization approaches.

The document is organized as follows: chapter 2 is devoted to the cost and power consumption model for the transceivers and ROADMs, with a special emphasis on the study of the DSP complexity and its translation to power consumption, as indicated above. The network-level performance evaluation is presented in chapter 3 for a reference national network topology. Finally, in chapter 4, we present our conclusions.

2. Cost and power consumption reference model

This chapter sums up the transceiver designs for different benchmarking implementations based on optical and electrical multiplexing schemes as well as the transceiver implementations proposed in the ASTRON project. These designs are used to estimate the cost and power consumption of the modules for the techno-economic evaluation presented in chapter 3. We also carry out a DSP power consumption evaluation based on ASIC- and FPGA-technology computational complexity, as well as a sensitivity analysis to estimate the transceiver cost and power elasticity to the cost and power consumption of relevant components.

2.1 Single-carrier and common multi-carrier transceiver implementations

In this section we present the designs of single-carrier and common multi-carrier transceivers and estimate the cost and power consumption of the modules. Furthermore, we include a transceiver market update and report on the progress of the standardization of 400G implementations.

2.1.1 Single-carrier transceiver

In Figure 2.1 we show a design of a single-carrier transceiver based on the OIF implementation agreements for 100G integrated polarization multiplexed quadrature modulated transmitter and intradyne coherent receivers, OIF-PMQ-TX-01.1 [2] and OIF-DPC-RX-01.2 [3], respectively. This transceiver will be used for the benchmarking cases (both in the single line rate (SLR) and multiple line rate (MLR) scenarios) explained in section 3.3. It consists of:

- a DSP chip (40 nm) with
  - four low frequency RF power dividers ($1k-$1.5k and 2-10W depending on the frequency range and on included amplifiers for loss compensation, if considered separately)
  - four DAC/ADC (1.5W per DAC/ADC for integrated solution and 2W for standalone solution. The DAC should be running at 64GSa/s)
- a four-port RF amplifier as modulator drivers
- four RF LP filters after the modulator drivers to remove the aliasing components. These can be dispensed with if the sampling rate of the DSP chip is sufficiently high in comparison with the electrical bandwidth. Additionally, four optional RF LP filters can be used in front of the ADCs, depending on the sampling rate and electrical bandwidth of the ADCs, to remove unwanted spectral components. An increased sampling rate of the ADCs would allow getting rid of the aliasing spectra in the DSP, but it would come at the price of increasing the amount of data to be processed at the receiver. We have considered RF LP filters both at the transmitter and the receiver.
- one polarisation-multiplexed IQ modulator
- two narrow-linewidth lasers (one at the transmitter and the other one at the receiver)
- one integrated, dual-polarisation coherent receiver, including a 90º hybrid, four balanced photodiodes and four transimpedance amplifiers (TIA)

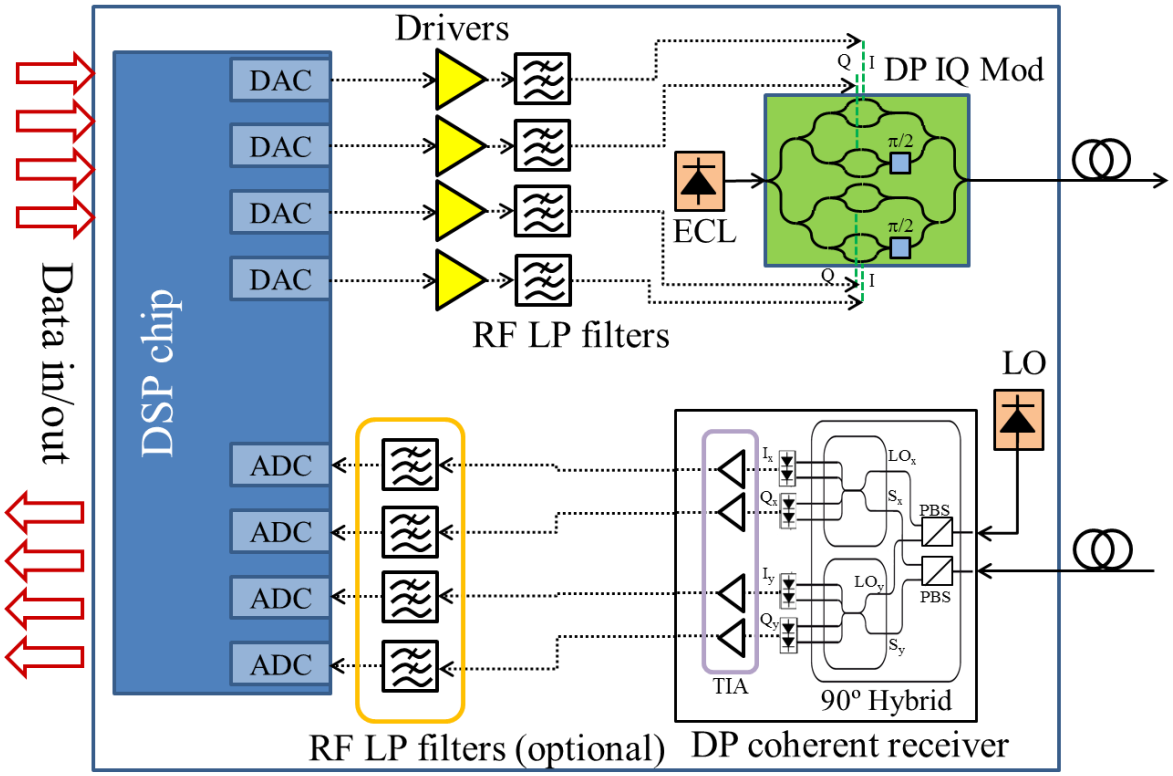


Figure 2.1 Design of a single-carrier transceiver for SLR and MLR.

Table 2.1 shows the cost and power consumption associated with the single-carrier transceiver depicted in Figure 2.1. The cost is expressed in absolute values (k$) and also relative to the cost of the 100G transceiver (*) or the 10G transceiver (**). The cost of the DSP excludes the development cost. It includes analogue front-end, i.e. 4× ADC and 4× DAC (64GSa/s) as well as first stage of AGC amplification and 4× low frequency RF power dividers. The power consumption of the DSP/FEC <35W, that of the four ADC/DAC is 1.5W, and that of the four power dividers equals 0.5 W.

Table 2.1 Relative cost and power consumption of a single-carrier transceiver to be used in the SLR and MLR benchmarking scenarios. (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver.

Component	Relative Unit cost (*)	Power (W) [max]	#	Relative cost (*)	Relative cost (**)	Total power (W)
DSP Chip	0.36	38.5	1	0.36	1.9	38.5
PM IQ Mod	0.22	0.0	1	0.22	1.1	0.0
Laser (Tx & Rx LO)	0.05	1.5	2	0.11	0.3	3.0
4-Port Modulator Driver	0.07	6.0	1	0.07	0.4	6.0
RF LP filter	0.004	0.0	8	0.03	0.0	0.0
DP Coherent Receiver	0.22	1.5	1	0.22	1.1	1.5
				1.00	5.2	49.0

The DSP cost can vary from 20% to >50% of the 100G transceiver cost (in our cost model it is ~36%) depending on whether or not systems vendors have in-house DSP chip development capability (see

Table 2.2). But other factors, which might enable a direct transceiver cost/power consumption reduction or an improved transmission performance, must also be taken into account:

- Low-power 20-nm ASIC
- 16-nm CMOS on the way (after 2016?)
- NL-effect compensation
- Stronger SD FEC (10 dB OSNR improvement for 100G DP-QPSK)
- Robust cycle-slip mitigation
- Interoperability features (e.g. Standard HD FEC)

Table 2.2 DSP ownership.

	In-house DSP	3rd party DSP/Module
Vendors	Alcatel-Lucent Ciena Cisco Huawei Infinera	ADVA BTI Coriant Cyan ECI Ericsson Fujitsu Huawei NEC Transmode Xtera ZTE
Shipment	85% of hardware shipped to date	NEL-based discrete designs and Acacia modules

(Source: Infonetics Research, 2014)

In metro networks, 100G "low-cost" and "energy-efficient" coherent PDM-QPSK pluggable interfaces are promised to a big success, and will not be replaced soon. System designers are interested to move to pluggable transceivers for 100G coherent applications to take advantage of the "pay as you grow" benefits and are urging for smaller transceivers in order to increase the bandwidth density. The CFP2 form factor has thus become very attractive, but faces the problem that the current technology cannot integrate all the necessary elements for a 100G coherent transceiver within either the footprint or the electrical power budget of a CFP2. A solution to the problem was to define a new type of coherent transceiver, the CFP2-ACO (analog coherent optics) [4], which removes the DSP ASIC from the module and places it on the line card. Its footprint is therefore reduced and it requires less power than alternative options such as the CFP or the OIF MSA, but reduces flexibility since CFP2-ACO can only be plugged into line card slots specifically designed for this transceiver technology. The CFP2-ACO transceiver has been recently announced or already released by several vendors (e.g. Fujitsu [5], NEC [6], Oclaro [7]) and is expected to be increasingly commonplace from 2016 onward. The CFP4-ACO, exhibiting further footprint and power reduction, is forecast to be released after 2018.

The CFP2-DCO (digital coherent optics), which does incorporate the DSP chip (thereby solving the flexibility problem of the CFP2-ACO), could be released in 2017, but this depends on competition from the ACO solution. In this scenario, market opportunities among system vendors without in-house ASIC capability need to be found. Recently, NTT, in collaboration with Broadcom Corporation, has started shipping the first 20-nm low-power coherent DSP, NLD0640 Gen2 LP-DSP. This makes merchant Silicon DSP solution available for all manufacturers and enables interoperability among multi-source pluggable coherent optics using lower-cost technologies such as compound semiconductor and silicon photonics [8]. NTT demonstrated successful interoperability of the new NLD0640 Gen2 LP-DSP not only with multi-source CFP2-ACOs but also with CFP-DCOs employing their own in-house DSP ASIC [9].

TEI contributed to the ITU-T discussion for G.698.2 "black link applications" with a work titled "Multi-vendor 100G DP-QPSK transmission experiment" (Turin, 12 –15 October 2015). This contribution reports the results of a successful multi-vendor transmission experiment between two different CFP implementations of a 100G DP-QPSK transceiver. The two CFP modules were based on two radically

different implementations, one being based on a photonic integrated circuit and the other being made of discrete components. The aim of this contribution was to share the conditions that enabled transverse compatibility of the two transceivers.

Regarding bit rates beyond 100G, 200G/400G DWDM transceivers, seeking 100G DCO compatibility, are now in production. According to the OIF white paper OIF-Tech-Options-400G-01.0 [10], single-carrier transceiver implementations are the preferred solutions for short-haul and metro applications, with baud rates ranging between 42.7 and 64 GBaud and high-level modulation formats (16QAM and above) with 50 to 75 GHz channel spacing, achieving spectral efficiencies above 5.3 bit/s/Hz. Compared with multi-carrier solutions, single-carrier solutions provide the benefit of a simple structure, easy wavelength allocation and network management, smaller size, lower power dissipation, and lower cost. The real challenge is the ADC due to the high requirements regarding bandwidth and effective number of bits (ENOB) for multi-level modulation. The ASIC design is also very difficult. Considering 8-bits quantization, the throughput would reach 4 Tb/s, in real time. Large-scale parallel process and fine clock control is required. At ECOC 2015, NTT announced the shipment of the industry-first 20nm CMOS coherent DSP providing 200 Gb/s 16QAM DSP for metro-access [11].

2.1.2 Multi-carrier transceivers

Even though higher bit rates per transceiver can be achieved in a single-carrier configuration by increasing the modulation level (thereby increasing the spectral efficiency, at the price of reducing the transmission reach) and the baud rate (which results in increased non-linear impairments and component requirements), the most viable solution is to resort to multi-carrier or super-channel transmission, whereby a signal is divided into sub-channel constituents at a lower baud rate and modulation level by means of compact multiplexing techniques such as Nyquist WDM (NWDM) or OFDM. Table 2.3 summarises several 400G transceiver implementations for short-haul (SH), metro, long-haul (LH) and ultra-long-haul (ULH) applications according to OIF-Tech-Options-400G-01.0 [10], including the DAC/ADC requirements and the maximum achievable reach. Table 2.4 shows in turn the OSNR requirements for different modulation formats and net bit rates per carrier. We observe that single-carrier implementations require not only higher electrical bandwidth (>25 GHz) and ENOB (>6), but also OSNR above 22dB for BER equal to 10^{-3}. For multi-carrier implementations, on the other hand, these requirements can be relaxed depending on the actual architecture, e.g. to reduce the OSNR required for a particular modulation format, the baud rate needs to be reduced (see Table 2.4). In any case, moving to 400G solutions faces a trade-off between spectral efficiency and reach flexibility.

If higher modulation levels are employed, reduced transmission reach is unavoidable because these high-order QAMs require higher OSNR, and are more sensitive to laser phase noise (e.g. 16QAM is 4-fold more sensitive than QPSK) and to fibre non-linear effects, in particular to non-linear phase noise. Similarly, the higher the QAM order, the lower the tolerance to narrow optical filtering due to ROADM cascading is [10].

Equipment suppliers seem today to converge towards super-channels composed of 2 sub-carriers carrying each 200G PDM-16QAM in 75 GHz bandwidth. When compared to 100G PDM-QPSK, the 2x200G PDM-16QAM requires 7 dB higher OSNR, which represents a reduction by a factor of ~5 of the maximum transmission distance [10]. Table 2.5 summarizes the main features of the 400G solutions proposed by equipment suppliers. 32 Gbaud seems to be the best trade-off to increase the spectral efficiency without stressing too much the electronics (DAC/ADC/RF drivers) or the transmission performance [10]. Another solution to the reach/spectral efficiency trade-off could be the use of hybrid Raman/EDFA amplification with improved noise figure.

Table 2.3 Potential 400G architectures in the state of the art. [1]DAC and ADC characteristics taken either from Section 6 or from the state of the art. [2]Distances reported either in the state of the art or from OIF contributions. [3]OIF2014.030.00, [4]OIF2015.030.01, [5]OIF2015.100.00, [6]OIF2015.037.01, [7]OIF2014.031.00 [10].

	Modulation	Symbol Rate (Gbaud)	#sub-channels	DAC Options[1]	ADC Options[1]	State of the art Distance (km)[2]
SH (~100 km, 50 GHz)	64QAM	42.7	1	1x4 80 GSa/s, 6.5 bits, 25 GHz[3]	1x4 80 GSa/s, 6.5 bits, 25 GHz[3]	300[Buchali 14]
	16QAM	64	1	1x4 88 GSa/s, 16 GHz[Rios-Muller 14]	1x4 90 GSa/s, 25 GHz[Rios-Muller 14]	6600[Rios-Muller 14]
Metro (<1000 km, 75/100 GHz, 10x ROADM)	16QAM	32	2	2x4 64 GSa/s, 16 GHz[4]	2x4 80 GSa/s, 33 GHz[4]	1800[4]
	16QAM	64	1	1x4 88 GSa/s, 16 GHz[Rios-Muller 14]	1x4 80 GSa/s, 33 GHz[Rios-Muller 14]	6600[Rios-Muller 14]
	64QAM	14.2	3	3x4 32 GSa/s, 6.5 bits, 10 GHz[5]	3x4 32 GSa/s, 6.5 bits, 10 GHz[5]	600[5]
	MB-OFDM (16QAM)	8	8	8x4 12 GSa/s, 10 GHz[Pincemin 14]	8x4 50 GSa/s, 5 GHz[Pincemin 14]	1000[Pincemin 14]
LH (~2000 km, optional ROADM)	QPSK	64	2	2x4 90 GSa/s, 5 bits, 20 GHz[6]	2x4 90 GSa/s, 5 bits, 20 GHz[6]	6577[Wang 15]
	QPSK	32	4	4x4 64 GSa/s, 14 GHz[7]	4x4 80 GSa/s, 33 GHz[7]	2975[7]
	16QAM	16	4	4x4 32 GSa/s, 5 bits, 10 GHz[3]	2x4 64 GSa/s, 5 bits, 17 GHz[3]	630[3]
ULH (>2000 km)	QPSK	32	4	4x4 64 GSa/s, 14 GHz[7]	4x4 80 GSa/s, 33 GHz[7]	2975[7]
	8QAM	42.7	2	2x4 64 GSa/s, 16 GHz[4]	2x4 80 GSa/s, 33 GHz[4]	6787[SZhang 14]
	16QAM	21	3	3x4 40 GSa/s, 6 bits, 11 GHz[5]	3x4 40 GSa/s, 6 bits, 11 GHz[5]	5000[5]

Table 2.4 OSNR requirements (theory) for 400G modulation format options. Achievable OSNR without decreasing net bit rate is highlighted in bold text. The net bit rate shown is per carrier [10].

Modulation Format	Net Bit Rate (Gb/s)	Symbol Rate (Gbaud)	Shaping	BW (GHz)	Grid (GHz)	SE (bit/s/Hz)	OSNR BER=10^{-3}	OSNR BER=10^{-2}
PDM-QPSK	100	28	NRZ	56	50	2	**12**	9.8
	100	32	Nyquist	35	50	2	12.6	**10.4**
	200	56	NRZ	112	100	2	**15**	12.8
	200	64	Nyquist	70	75	2.66	15.6	**13.4**
PDM-8QAM	100	18.7	NRZ	37.3	50	2	**13.8**	11.4
	100	21.3	Nyquist	23.4	25	4	14.3	**12**
	200	37.3	NRZ	74.6	100	2	**16.8**	14.4
	200	42.7	Nyquist	47	50	4	17.4	**15**
PDM-16QAM	100	16	Nyquist	17.6	25	4	16.2	**13.8**
	200	32	Nyquist	35.2	50	4	19.2	**16.8**
	400	64	Nyquist	70.4	75	5.33	22.2	**19.8**
PDM-64QAM	200	21.3	Nyquist	23.4	25	8	23.4	**20.8**
	400	42.7	Nyquist	47	50	8	26.4	**23.8**

Table 2.5 Proposed 400G WDM transmission solutions [10].

Modulation	QPSK	16QAM	16QAM	8QAM	QPSK	QPSK
Overall Data Rate (Gb/s)	100	400	400	400	400	400
Symbol Rate (Gbaud) with FEC	32	32	64	43	64	32
Number of sub-channels	1	2	1	2	2	4
Nyquist filtering	No	Yes	Yes	Yes	Yes	Yes
Data rate per sub-channel (Gb/s)	100	200	400	200	200	100
Channel occupancy (GHz)	50	75	75	100	150	150
SE (bit/s/Hz)	2	5.33	5.33	4	2.66	2.66
Required OSNR at BER=10^{-2}	12.5	19.5	22.5	18.5	13.4	12.5
Maximum transmission reach* (km)	~2000	~400	~200	~500	~600	~2000
HW implementation penalty		++	+++	+++	++	+

From the carriers point of view, the reach for LH should be >2,000 km, and the reach for metro and regional >1,000 km. Furthermore, a 4x100G implementation is perceived to be more flexible than a 2x200G or 1x400G. Regarding the 2x200G PDM-16QAM implementation at 32 Gbaud, it can be fitted in a 75 GHz spectral slot according to ITU-T G694.1 flex-grid, but there are concerns about the filtering penalties arising from transmission over cascaded ROADMs, since ~10 ROADMs are required. Keeping the 50-GHz ITU-T grid for 400G transmission seems pragmatic, and this can be advantageous for the frequency-packing flexible approach supported by Ericsson.

Finally, regarding standardization –and on account of the great number of proposed 400G solutions (cf. Table 2.3 and Table 2.4)–, it is important that the "modulation format soup" that "killed" the 40G data-rate should not be reproduced at 400G. Similarly, a 400G client physical interface needs to be standardized. IEEE 802.3 launched the 400GbE task force (IEEE 802.3bs [12]) in March 2014. The 802.3bs study group has converged to a common transmission technology (PAM-4) for applications 400GBASE-DR4, LR4, FR4, with the following specifications:

- DR4: 4 parallel duplex SMF, each carrying 100G, at 56Gbaud/s PAM-4, 500m
- LR8: 1 duplex SMF with 8×50G LANWDM wavelengths, each carrying 28Gbaud/s PAM-4, 10km
- FR8: same technology of LR8, de-spec'd for 2km reach

According to the IEEE 802.3bs 400GbE Task Force timeline adopted in September 2015, the standard is expected in December 2017 [12].

In the following subsections we review several multi-carrier transceiver solutions, implementing either electrical multiplexing schemes, such as eOFDM, Nyquist WDM with digital filtering (NFDM) and the ASTRON project solution based on optical sub-banding –OS-OFDM–, or optical multiplexing schemes, such as Nyquist WDM with optical filtering (NWDM) and AO-OFDM. Based on the carriers' needs summarised above, we focus on *N*×100G configurations at 32GBaud (where *N* is the number of sub-channels) to provide greater flexibility and the transmission reaches required by LH/ULH applications.

2.1.2.1 eOFDM/NFDM super-channel transceiver

Figure 2.2 shows the design of a super-channel transceiver for the electrical multiplexing schemes (eOFDM and Nyquist-WDM with digital filtering). It employs a comb generator modulator driven by a sinusoidal signal, two AWGs, an N:1 combiner and a 1:N splitter. The AWGs should exhibit a similar filtering performance throughout the C-band. Alternatively, the optical sub-carrier multiplexing can be

made external to the super-channel transceiver, as explored in IDEALIST and SPIRIT projects. We have assumed for the cost and power consumption evaluation that the maximum number of sub-channels is 8.

In the cost model presented in Table 2.6 we have assumed a reduction of 40% in the cost of all components, except for the DSP, accounting for electronic integration, including integrated photonic circuit development, integration with active and passive RF electronics, as well as packaging savings of the integrated transceiver with respect to eight single-carrier transceivers. In an alternative design, the variable gain dual-stage amplifier may not be integrated for practical reasons, in which case the integration reduction factor would not affect this component and the overall cost of the super-channel transceiver would be 6.0 times the cost of a 100G transceiver or 31.4 times the cost of a 10G transceiver (i.e. 1.2% more expensive).

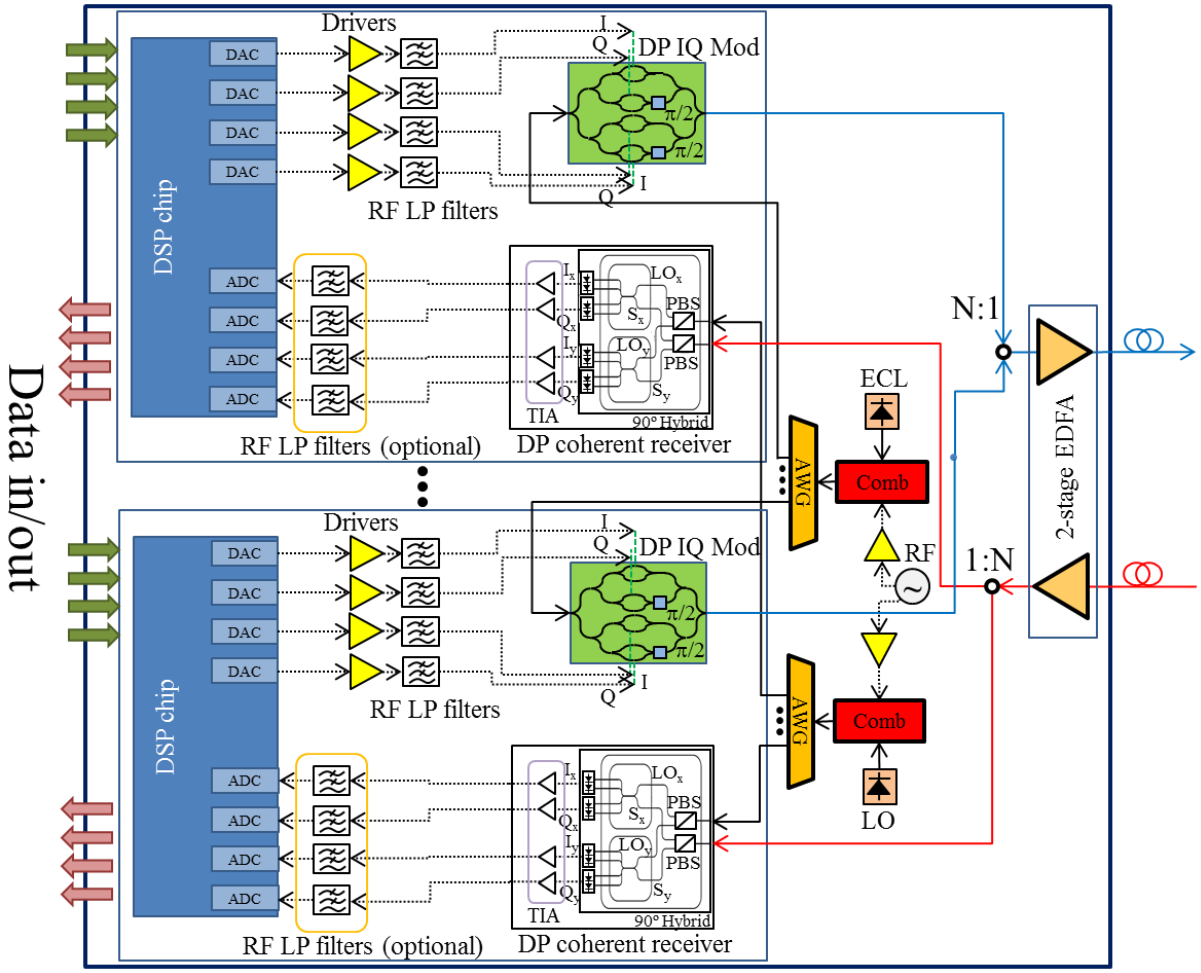


Figure 2.2 Design of a super-channel transceiver for the eOFDM and Nyquist-WDM (with digital filtering) schemes.

Table 2.6 Relative cost and power consumption of a super-channel transceiver for the eOFDM and NWDM with digital filtering. (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver.

Component	Relative unit cost (*)	Power (W) [max]	#	Relative total cost (*)	Relative total cost (**)	Total power (W)
DSP Chip	0.36	38.5	8	2.88	15.04	308.0
PM IQ Mod	0.22	0.0	8	1.04	5.41	0.0

Laser (Tx & Rx LO)	0.05	1.5	2	0.06	0.34	3.0
4-Port Modulator Driver	0.07	6.0	8	0.35	1.80	48.0
RF LP filter	0.00	0.0	64	0.14	0.72	0.0
DP Coherent Receiver	0.22	1.5	8	1.04	5.41	12.0
Variable gain dual-stage amplifier	0.18	12.0	1	0.11	0.56	12.0
Comb generator modulator	0.18	0.0	2	0.22	1.13	0.0
Comb generator mod. driver	0.07	2.0	2	0.09	0.45	4.0
1:N AWG	0.02	0.0	2	0.02	0.11	0.0
				5.93	30.98	387.0

2.1.2.2 NWDM super-channel transceiver

In this type of transceiver implementation, the spectrum filtering is done in the optical domain, and therefore the RF LP filters are replaced with 1×1 high-spectral-resolution (HSR) filters [13], totally flexible in selecting any centre frequency in the C-band, followed by amplification stages to compensate for the power loss at the filters. Apart from that, there are no other major changes in the transceiver design with respect to the electrical multiplexing case presented in Figure 2.2. Figure 2.3 shows the super-channel transceiver design for NWDM with optical filtering. To reduce the cost, odd and even sub-channels are multiplexed separately and fed into two 1x1 HSR filters. An interleaver (ITL) is used to combine the two sets of sub-channels prior to amplification. Alternatively, a -3dB coupler can be used.

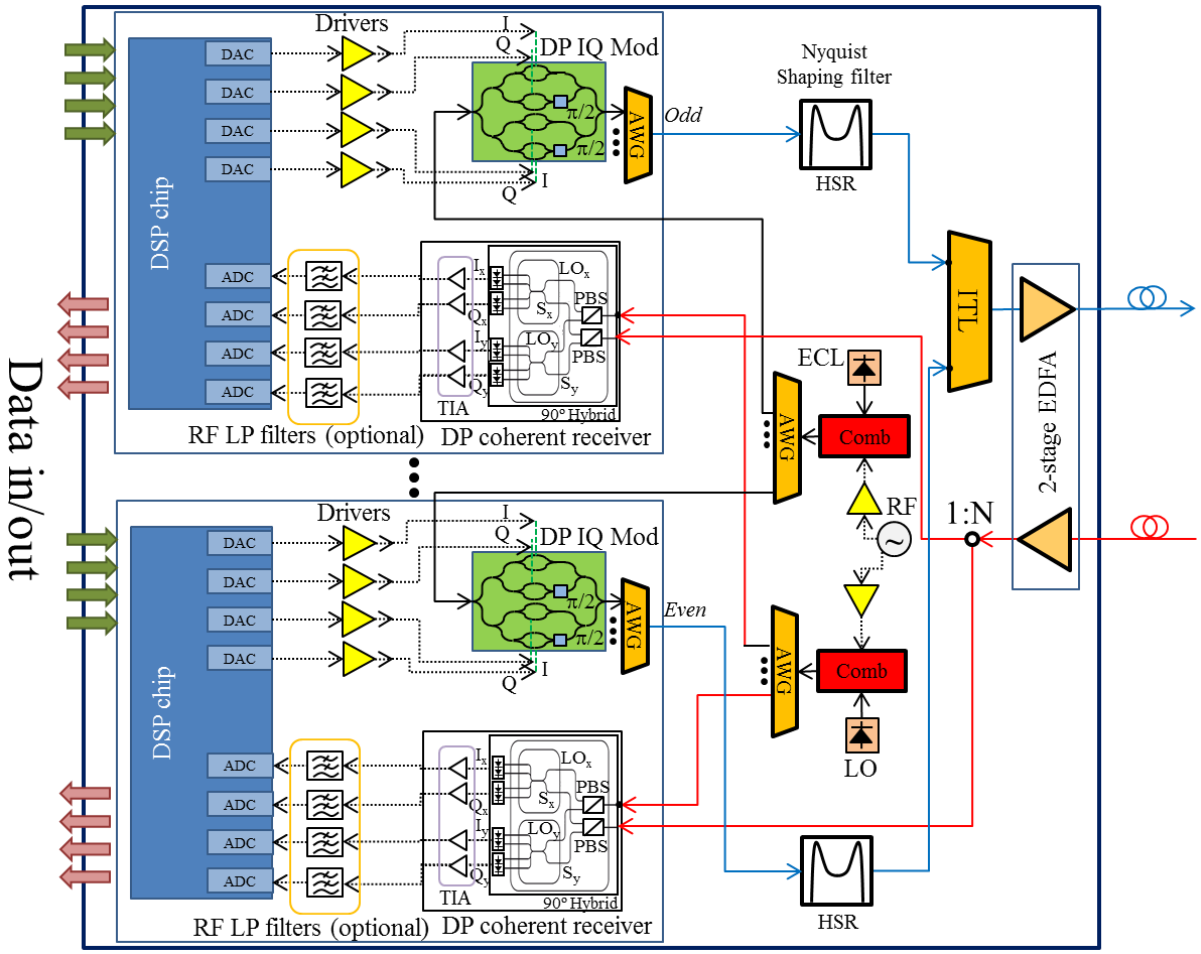


Figure 2.3 Design of a super-channel transceiver for the Nyquist-WDM (with optical filtering) scheme.

In Table 2.7 the cost and power consumption for the super-channel transceiver are presented. In this implementation, HSR filters are shared between even and odd sub-channels, so only two HSR filters are needed for the eight sub-channels. Compared with the super-channel transceiver for the electrical multiplexing schemes, the cost is less than 5% higher and the power consumption is ~2% higher. Note that in this design the DSP chip and the HSR filter do not benefit from a 40% cost reduction on account of the integration process. We can anticipate that further technology development may lead to the integration of both HSR filters (for even and odd sub-channels) in one, so only a single N×1 HSR filter (without interleavers and 1:N/M MUXs) would be required, with the associated cost and power consumption reduction. We can estimate the relative cost of an 8×1 scalable HSR filter to be 0.72 (with respect to the cost of a 100G transceiver). In this case, the relative total cost of the super-channel transceiver would come down to 30.3 times the cost of a 10G transceiver or 5.8 times the cost of a 100G transceiver and the power consumption would be 391W (instead of 395W), as shown in Table 2.8.

Table 2.7 Relative cost and power consumption of a super-channel transceiver for the NWDM with optical filtering, assuming two HSR filters are used, one for even sub-channels and another one for odd sub-channels. M: Number of Nyquist-shaping HSR filter per super-channel transceiver. N: Number of sub-channels per super-channel (i.e. 8). (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver.

Component	Relative unit cost (*)	Power (W) [max]	#	Relative cost (*)	Relative cost (**)	Total power (W)
DSP Chip	0.36	38.5	8	2.88	15.04	308.0

PM IQ Mod	0.05	0.0	8	0.26	1.35	0.0
Laser (Tx & Rx LO)	0.05	1.5	2	0.06	0.34	3.0
4-Port Modulator Driver	0.07	6.0	8	0.35	1.80	48.0
RF LP filter	0.00	0.0	32	0.07	0.36	0.0
DP Coherent Receiver	0.22	1.5	8	1.04	5.41	12.0
Variable gain dual-stage amplifier	0.18	12.0	1	0.11	0.56	12.0
Comb generator modulator	0.18	0.0	2	0.22	1.13	0.0
Comb generator mod. driver	0.07	2.0	2	0.09	0.45	4.0
1:N AWG	0.02	0.0	2	0.02	0.11	0.0
Interleaver	0.03	0.0	1	0.02	0.08	0.0
1:(N/M) MUX	0.02	0.0	2	0.02	0.11	0.0
1x1 HSR filter	0.54	4.0	2	1.08	5.64	8.0
				6.20	32.39	395.0

Table 2.8 Relative cost and power consumption of a super-channel transceiver for the NWDM with optical filtering, assuming one 1×N HSR filter per super-channel. N: Number of sub-channels per super-channel (i.e. 8). (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver.

Component	Relative unit cost (*)	Power (W) [max]	#	Relative cost (*)	Relative cost (**)	Total power (W)
DSP Chip	0.36	38.5	8	2.88	15.04	308.0
PM IQ Mod	0.05	0.0	8	0.26	1.35	0.0
Laser (Tx & Rx LO)	0.05	1.5	2	0.06	0.34	3.0
4-Port Modulator Driver	0.07	6.0	8	0.35	1.80	48.0
RF LP filter	0.00	0.0	32	0.07	0.36	0.0
DP Coherent Receiver	0.22	1.5	8	1.04	5.41	12.0
Variable gain dual-stage amplifier	0.18	12.0	1	0.11	0.56	12.0
Comb generator modulator	0.18	0.0	2	0.22	1.13	0.0
Comb generator mod. driver	0.07	2.0	2	0.09	0.45	4.0
1:N AWG	0.02	0.0	2	0.02	0.11	0.0
Nx1 HSR filter	0.72	4.0	1	0.72	3.76	4.0
				5.80	30.32	391.0

2.1.2.3 Conventional AO-OFDM super-channel transceiver

In Figure 2.4 we show the super-channel transceiver design for the AO-OFDM transmission scheme. Because as high a bandwidth as possible is needed, the RF low-pass filters are removed and so could the four DACs. However, in our current cost evaluation we are considering them for pre-emphasis of the electrical signal. The results of the cost and power consumption evaluation, shown in Table 2.9, are essentially the same as those for the super-channel transceiver for the electrical multiplexing schemes (the AO-OFDM transceiver is just ~1.2% more cost-effective).

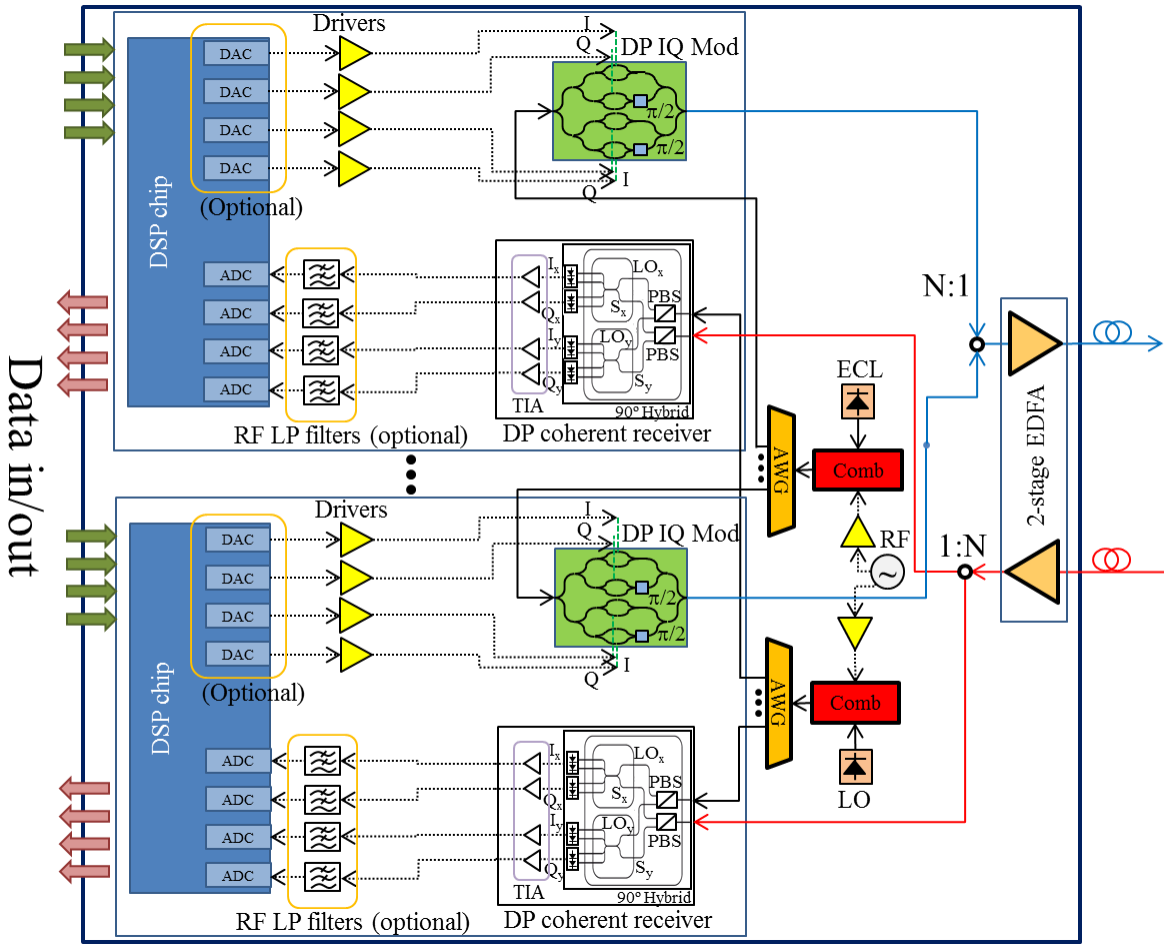


Figure 2.4 Design of a super-channel transceiver for the conventional AO-OFDM scheme.

Table 2.9 Relative cost and power consumption of a super-channel transceiver for the conventional AO-OFDM scheme. (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver.

Component	Relative unit cost (*)	Power (W) [max]	#	Relative cost (*)	Relative cost (**)	Total power (W)
DSP Chip	0.36	38.5	8	2.88	15.04	308.0
PM IQ Mod	0.22	0.0	8	1.04	5.41	0.0
Laser (Tx & Rx LO)	0.05	1.5	2	0.06	0.34	3.0
4-Port Modulator Driver	0.07	6.0	8	0.35	1.80	48.0
RF LP filter	0.00	0.0	32	0.07	0.36	0.0
DP Coherent Receiver	0.22	1.5	8	1.04	5.41	12.0
Variable gain dual-stage amplifier	0.18	12.0	1	0.11	0.56	12.0
Comb generator modulator	0.18	0.0	2	0.22	1.13	0.0
Comb generator mod. driver	0.07	2.0	2	0.09	0.45	4.0
1:N AWG	0.02	0.0	2	0.02	0.11	0.0
				5.86	30.62	387.0

2.2 ASTRON super-channel transceiver implementations

In this section we present the designs of the super-channel transceivers proposed in the ASTRON project and we estimate the cost and power consumption of the modules. This is followed by a DSP power consumption evaluation based on ASIC- and FPGA-technology computational complexity.

2.2.1 AO-OFDM transceiver

The key features of the ASTRON transceiver are the energy-efficiency and bit-rate flexibility to support rates from 10Gb/s to beyond 1Tb/s, for use in both access and core networks. To achieve energy efficiency, the ASTRON transceiver does not implement the discrete Fourier transform (DFT) in the electric domain, using power-consuming DSP and ADCs, but uses a specially designed AWG to multiplex and de-multiplex AO-OFDM and Nyquist-WDM signals directly in the optical domain, as depicted in Figure 2.5.

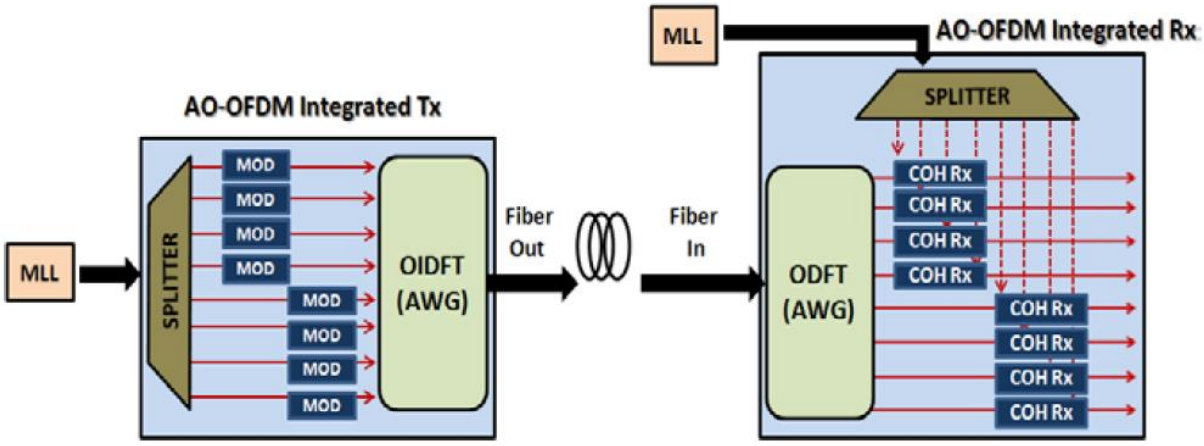


Figure 2.5 Scheme of ASTRON's AO-OFDM scheme (from D2.4).

In this report, we consider the AO-OFDM system performance in access/metro and core networks separately. In the first case, the link length is limited to 100 km, without chromatic dispersion compensation and using single polarization and direct detection (DD) to comply with all the existing (and coming soon) passive optical network (PON) standards.

In addition, we consider an AO-OFDM transceiver implementation for core networks that incorporates a coherent receiver and a DSP.

2.2.1.1 AO-OFDM super-channel transceiver without DSP

In OFDM, time gating is necessary to sample the received optical symbol at the DFT point, so that all the contributions from the other OFDM subcarriers are eliminated. To sample the optical signals received at the AWG output ports, a set of time gating devices are required, which, in the ASTRON project, are pulsed LOs, as discussed in D2.3.

The setup of the AO-OFDM system investigated is shown in Figure 2.6. At the OLT side, the source signal is an optical comb with Gaussian pulses, followed by an optical band-pass filter and a splitter. The optical pulses enter a set of optical modulators, where downstream signals are applied by each operator. We consider phase-modulator for differential phase shift keying (DPSK) modulation and differential quadrature phase shift keying (DQPSK) modulation.

The IDFT/DFT operation is performed in the optical domain by the AWG. Alternatively, it is possible to use a wavelength selective switch (WSS) at the OLT side, in order to make a flexible assignment of the subcarriers to different operators.

The AWG has 16 ports, 12.5 GHz subcarrier spacing and 200 GHz free spectral range. We can consider data rates Rs=12.5 Gb/s and Rs=10 Gb/s for each ONU. In the first case, we have a capacity of 16 x 12.5 = 200 Gb/s for the DPSK modulation and 400 Gb/s for DQPSK modulation, and the spectral bandwidth

is 200 GHz. In the second case, for the same spectral bandwidth, the overall capacity is 16 x 10 = 160 Gb/s for DPSK modulation and 320 Gb/s for DQPSK modulation. At the RN, the AWG device demodulates the information symbols, and each output is connected to a different ONU. At the receiver (Rx), the optical gate samples the signal in the middle of the eye diagram, and an one bit delay line interferometer (DLI) followed by a balanced photo-detector (BPD) receives the user data stream. In the numerical simulations, we have considered an optical pre-amplifier at the receiver side, and the received power is evaluated as a function of the optical signal to noise ratio (OSNR). The amplifier noise figure is 5 dB.

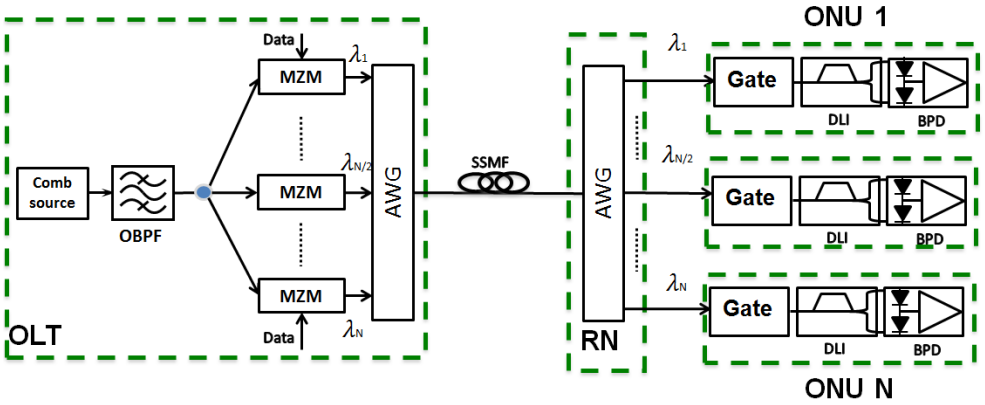
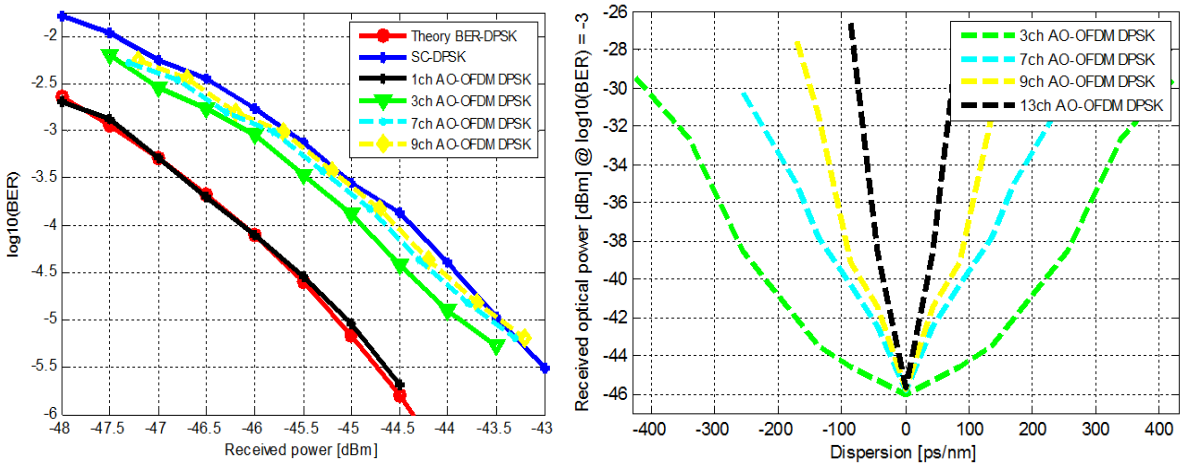


Figure 2.6 Design of an ASTRON AO-OFDM transceiver without DSP for access networks.

In the following simulations, we have considered an optical Gaussian filter with optical bandwidth equal to 2*Rs, and an electrical 5-th order Bessel filter, with 0.8*Rs bandwidth. We have estimated the average bit error rate (BER) by Monte Carlo (MC) simulations, for only the central subcarrier. The BER accuracy is 0.1 bit, with 64% Gaussian confidence. Figure 2.7(a) shows the BER for a back-to-back (BtB) configuration for 12.5 Gb/s DPSK modulation. In blue-line is shown the performance of a single carrier 12.5 Gb/s DPSK modulated, without time-gating, and in red-line is shown the theoretical curve of DPSK modulation. In black-line is shown a single carrier DPSK AO-OFDM modulated with same performance as the theoretical one, because we are receiving with a match filter. We also show the performance in the case of 3, 7, 9 channels DPSK AO-OFDM, which show better performance in BtB compared to single channel DPSK. At a log(BER) equal to -3, we find a 2.5dB penalty compared to the theoretical one due to the cross-talk between the channels. To measure the system performance, in terms of chromatic dispersion (CD) tolerance, we change the length of the SMF, in order to get different values of CD. We have not considered polarization mode dispersion (PMD) or nonlinear effects. Figure 2.7(b) shows the CD tolerance at 12.5 Gb/s for different numbers of ONU. We show the received optical power at a log(BER) equal to -3 as a function of the total accumulated CD. As can be observed, the system shows large penalty if we increase the number of ONU. If we consider adding a cyclic prefix (CP) to the signal, we can increase the CD tolerance as shown in Figure 2.8. We consider just 20% of CP, corresponding to 10 Gb/s for each ONU.



(a) (b)

Figure 2.7 (a) BER as a function of the received power for a 12.5 Gb/s DPSK AO-OFDM subcarrier in BtB for different number of channels. (b) Received optical power as a function of the total CD for a variable number of ONU.

As can be observed from the figure, we can further increase the CD tolerance. E.g. for the 13-ONU case we can reach approximately 20 km of SMF.

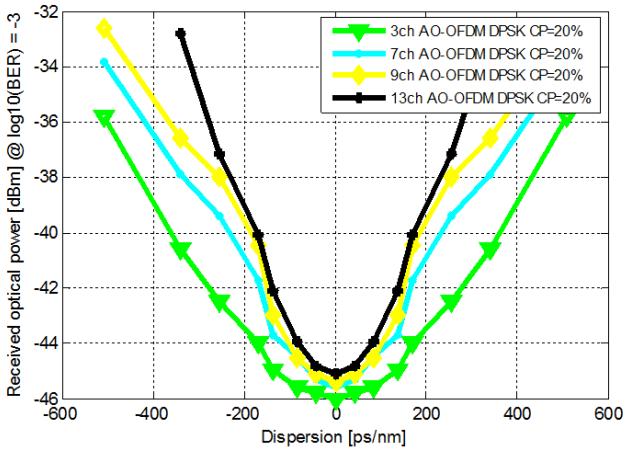


Figure 2.8 Received optical power as a function of the total CD for a variable number of ONU considering 20% of CP.

Moreover, we investigated the performance of DQPSK modulation for a bit rate equal to 25 Gb/s for each ONU. We show in Figure 2.9 the BER as a function of the received optical power in BtB. In blue-line is shown the performance of a single carrier 25 Gb/s DQPSK, in red line is shown the theoretical curve and in black line the 25 Gb/s DQPSK AO-OFDM single carrier. We observe the perfect match between the AO-OFDM and the theoretical curve because we are in the case of matched filter.

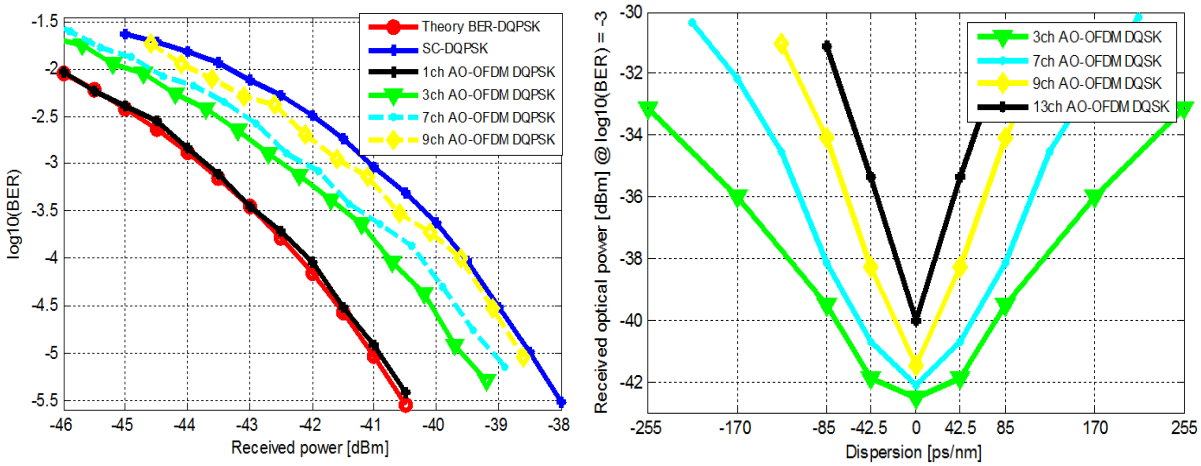


Figure 2.9 BER as a function of the received power for a 25 Gb/s DQSK AO-OFDM subcarrier in BtB for different number of channels. (b) Received optical power as a function of the total CD for a variable number of ONU.

There are 2 dB of penalty at log(BER) equal to -3 between the single-carrier DQPSK and the 1ch AO-OFDM. In the case of 3, 7 and 9 ONU this penalty becomes lower, so their performance in BtB is better than that of the DQPSK modulated without optical filters. In the case of 9 ONU we find a penalty of 2 dB due to the cross-talk of the adjacent channels.

To increase the dispersion tolerance, we consider 20% of CP and show the performance in Figure 2.10 for 3, 7, 9, and 13 ONU. The results show a received optical power of -32 dBm for a total CD of 170 ps/nm.

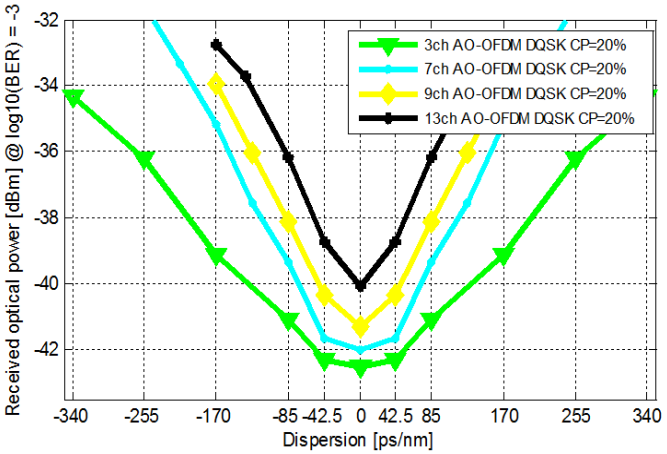


Figure 2.10 Received optical power as a function of the total CD for a variable number of ONU considering 20% of CP.

Table 2.10 Relative cost and power consumption of a super-channel transceiver for the AO-OFDM scheme with DD. (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver.

Component	Relative unit cost (*)	Power (W) [max]	#	Relative cost (*)	Relative cost (**)	Total power (W)
Modulator	0.14	0.0	8	1.18	6.4	0.0
Laser (Tx & Rx time-gate LO)	0.05	1.5	2	0.1	0.3	3.0
4-Port Modulator Driver	0.07	6.0	8	0.3	1.8	48.0
RF LP filter	0.00	0.0	32	0.1	0.4	0.0

BPDV	0.05	0.00	8	0.4	0.15	0.0
MZDI	0.01	0.0	8	0.08	1.14	0.0
Variable gain dual-stage amplifier	0.18	12.0	1	0.1	0.6	12.0
Comb generator modulator	0.18	0.0	2	0.2	1.1	0.0
Comb generator mod. driver	0.07	2.0	2	0.1	0.5	4.0
1:N AWG	0.02	0.0	2	0.0	0.1	0.0
				2.38	12.8	67

2.2.1.2 AO-OFDM super-channel transceiver with DSP at the receiver

The AO-OFDM scheme is shown in Figure 2.11.

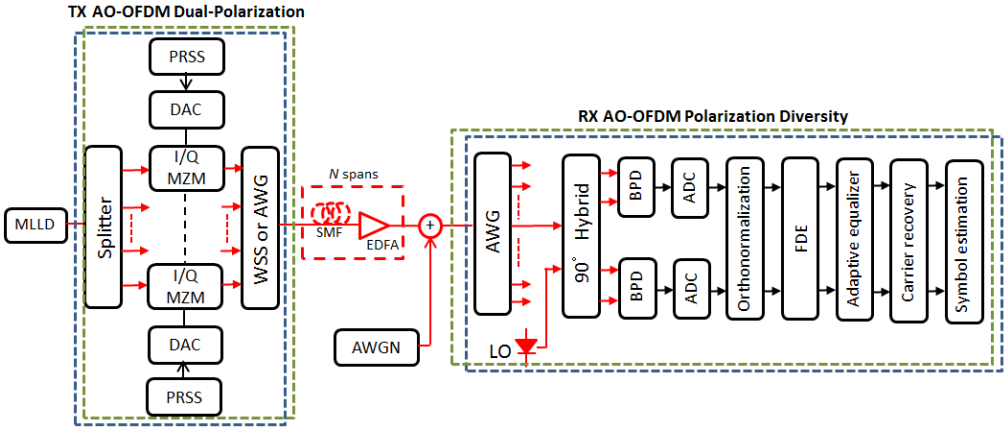


Figure 2.11 Scheme of an AO-OFDM transceiver with DSP at the receiver.

In the AO-OFDM scheme, the coherent Rx includes a CW laser as local oscillator (LO), a dual polarization 2×4 90^{o} hybrid coupler, and four balanced photodetectors (BPD). The received signals are filtered by a five-pole Bessel filter to simulate the Rx bandwidth limitation, and sampled with a 6-bit resolution by ADC.

The DSP consists of orthonormalization blocks, digital CD compensation based on an overlap-and-save frequency-domain equalization (FDE) filter, adaptive equalizer for the PMD, joint carrier recovery using a feed-forward carrier phase recovery (FFCPE) and maximum like-hood (ML) symbol detection.

Based on the schemes depicted in Figure 2.5 and Figure 2.11, we propose the AO-OFDM super-channel transceiver design shown in Figure 2.12 for core networks. The cost and power consumption model is presented in Table 2.11. The difference in power consumption between the ASTRON transceiver implementation and that for conventional AO-OFDM (Table 2.9) is due to the fact that DAC are not required in the ASTRON implementation. Despite that, the DSP is estimated to have the same cost.

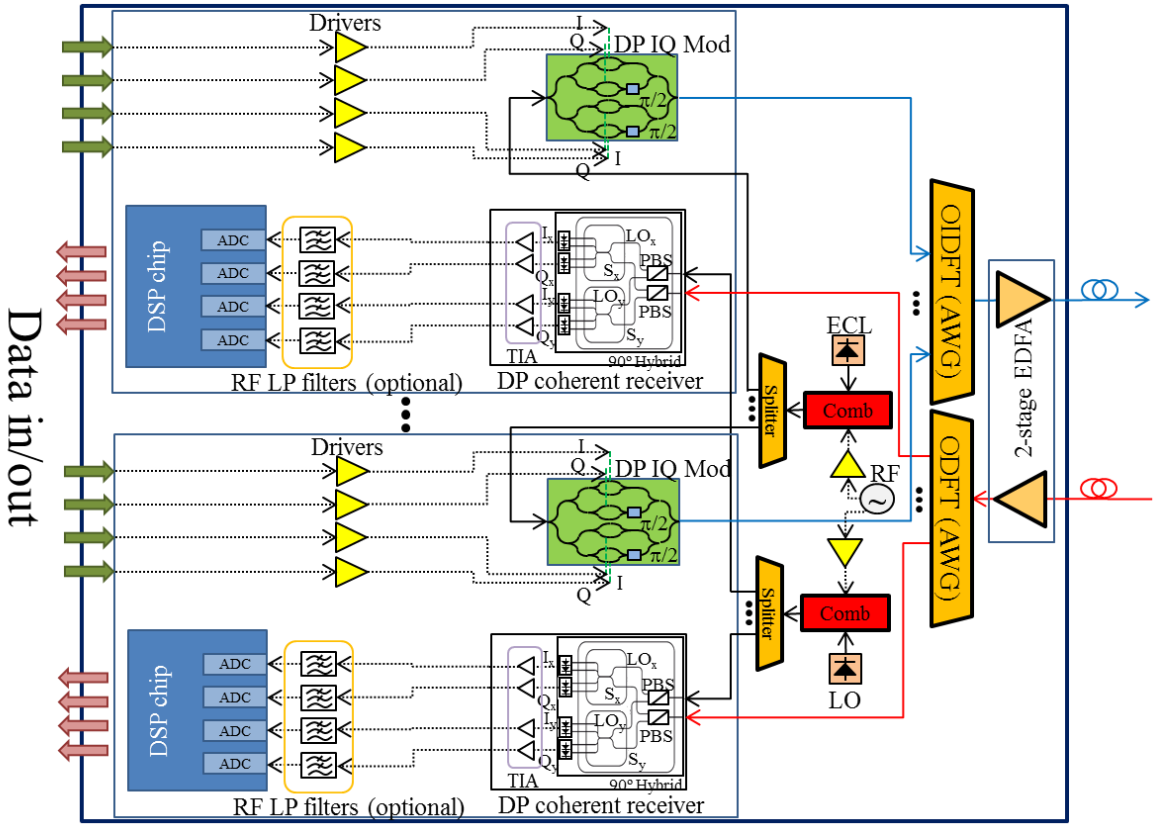


Figure 2.12 Design of an ASTRON AO-OFDM transceiver with DSP at the receiver intended for backbone networks.

Table 2.11 Relative cost and power consumption of a super-channel transceiver for the AO-OFDM scheme. (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver.

Component	Relative unit cost (*)	Power (W) [max]	#	Relative cost (*)	Relative cost (**)	Total power (W)
DSP Chip	0.36	37.0	8	2.88	15.04	296.0
PM IQ Mod	0.22	0.0	8	1.04	5.41	0.0
Laser (Tx & Rx LO)	0.05	1.5	2	0.06	0.34	3.0
4-Port Modulator Driver	0.07	6.0	8	0.35	1.80	48.0
RF LP filter	0.00	0.0	32	0.07	0.36	0.0
DP Coherent Receiver	0.22	1.5	8	1.04	5.41	12.0
Variable gain dual-stage amplifier	0.18	12.0	1	0.11	0.56	12.0
Comb generator modulator	0.18	0.0	2	0.22	1.13	0.0
Comb generator mod. driver	0.07	2.0	2	0.09	0.45	4.0
1:N AWG	0.02	0.0	2	0.02	0.11	0.0
				5.86	30.62	375.0

2.2.2 OS-OFDM transceiver

The OS-OFDM scheme features a multi-port optical comb generator (MPORT-OCG) generating the OFDM CW un-modulated sub-carriers. In ASTRON we propose to realize the MPORT-OCG as shown in Figure 2.13, using an MLL, a band-limiting optical filter (BL-OF) and an OIDFT device, realized by means

of an AWG. Alternatively, the MPORT-OCG can be realized using a CW laser followed by phase and amplitude modulators and an OIDFT device.

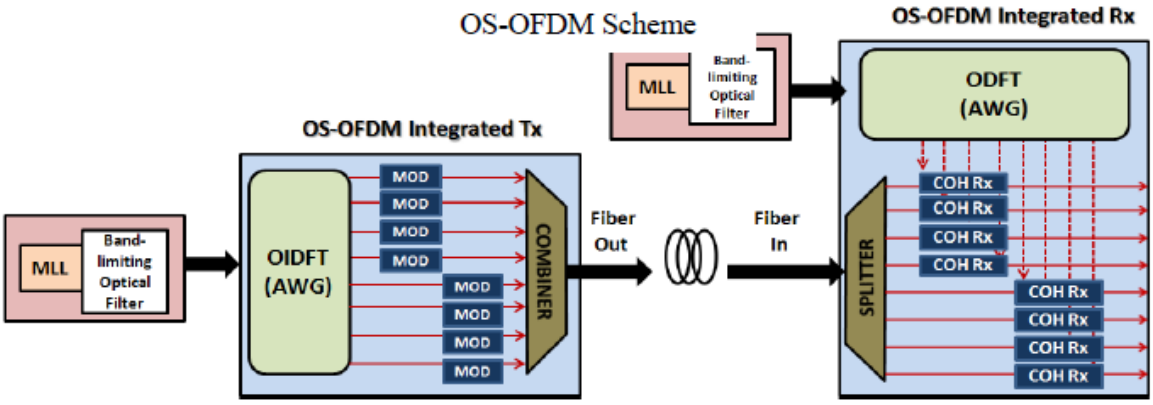


Figure 2.13 Scheme of the OS-OFDM (from D2.4).

The MPORT-OCG eight outputs feed an array of eight IQ modulators realized according to the ASTRON proposed InP technology. Each of the modulators is driven by a pair of DACs. The modulator outputs are passively combined in the COMBINER module to generate the Tx optical output. At the receiver, the signals are combined with LOs derived from a second OCG using 90° hybrids. For each channel, a polarization beam splitter is used to separate the two polarizations, and following balanced detection, the signals are digitised using ADCs. DSP is used at the transmitter to perform signal shaping (e.g. Nyquist pulse shaping using root-raised cosine filters, or orthogonal frequency division multiplexing), and at the receiver for dispersion and PMD compensation, polarization tracking, frequency and phase estimation.

Flexible optical transceivers (with reconfigurable rate and modulation format) may be efficiently realized using filter-bank-based digital sub-banding. The new ASIC architecture achieves record low complexity and high performance. The processing is partitioned into two tiers. The filter-bank top tier is hard-coded in high-speed hardware, whereas the bottom processing tier at ~1 GHz speed per sub-band may be flexibly implemented in an array of programmable DSP structures, readily reconfigurable and amenable to software upgrades as DSP algorithms evolve. In particular this DSP architecture supports the most hardware-efficient realizations of real-time full-functionality coherent OFDM transceivers to date.

Reduced-Guard-Interval (RGI) coherent optical OFDM is a leading method leveraging the spectral efficiency advantages of OFDM while mitigating the excessive penalty of the Cyclic Prefix (CP) overhead. We have recently proposed a new way to structure the digital signal processing (DSP) for RGI OFDM optical receivers: Multi-Sub-Band OFDM (MSB-OFDM). The idea is to break the digital processing into multiple parallel virtual sub-channels, occupying disjoint spectral sub-bands (Figure 2.14). E.g., in our favorite embodiment, in the receiver ASIC DSP, each sub-channel is digitally partitioned into 15 bands of ~1.6 GHz each. Remarkably, this digital de-multiplexing into sub-bands may be performed efficiently, with low computational complexity, with neither spectral guard-bands in between the 1.6 GHz bands nor with spectral guard-bands between the sub-channels. The new sub-banded optical receiver architecture is a significant enabler of flexibility and reconfigurability in coherent optical OFDM transceiver design, as explored in D2.4.

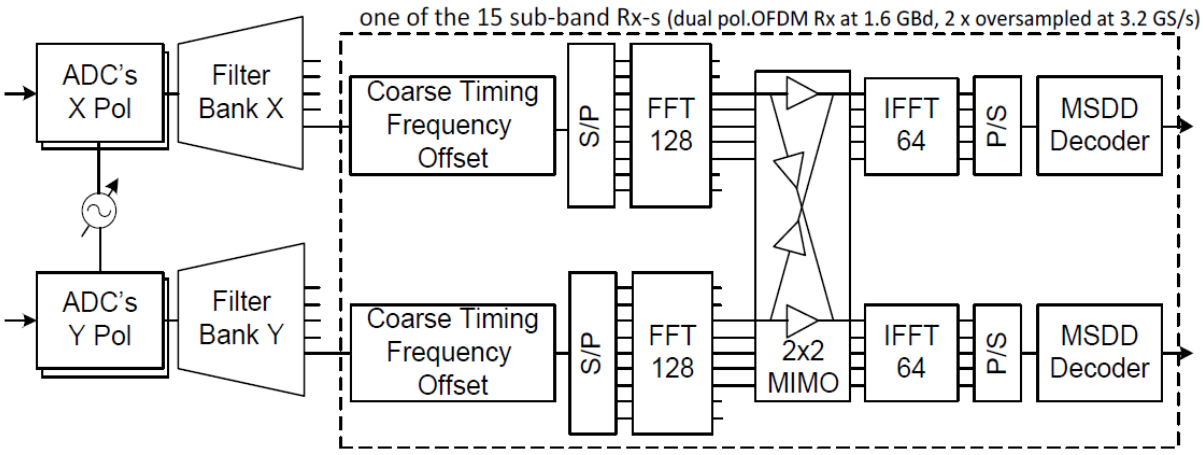


Figure 2.14 Basic MSB DFT-S OFDM receiver architecture, showing the two filter banks (one per polarization) and one of 15 sub-band receivers, fed by the corresponding index sub-bands of the X and Y polarizations (from D2.4).

In Figure 2.15 we show the design of the OS-OFDM implementation chosen for our cost and power consumption reference model. We have opted to realize the MPORT-OCG using a CW laser followed by phase and amplitude modulators, since that was the realization employed in the multi-carrier transceivers analysed in subsection 2.1.2.

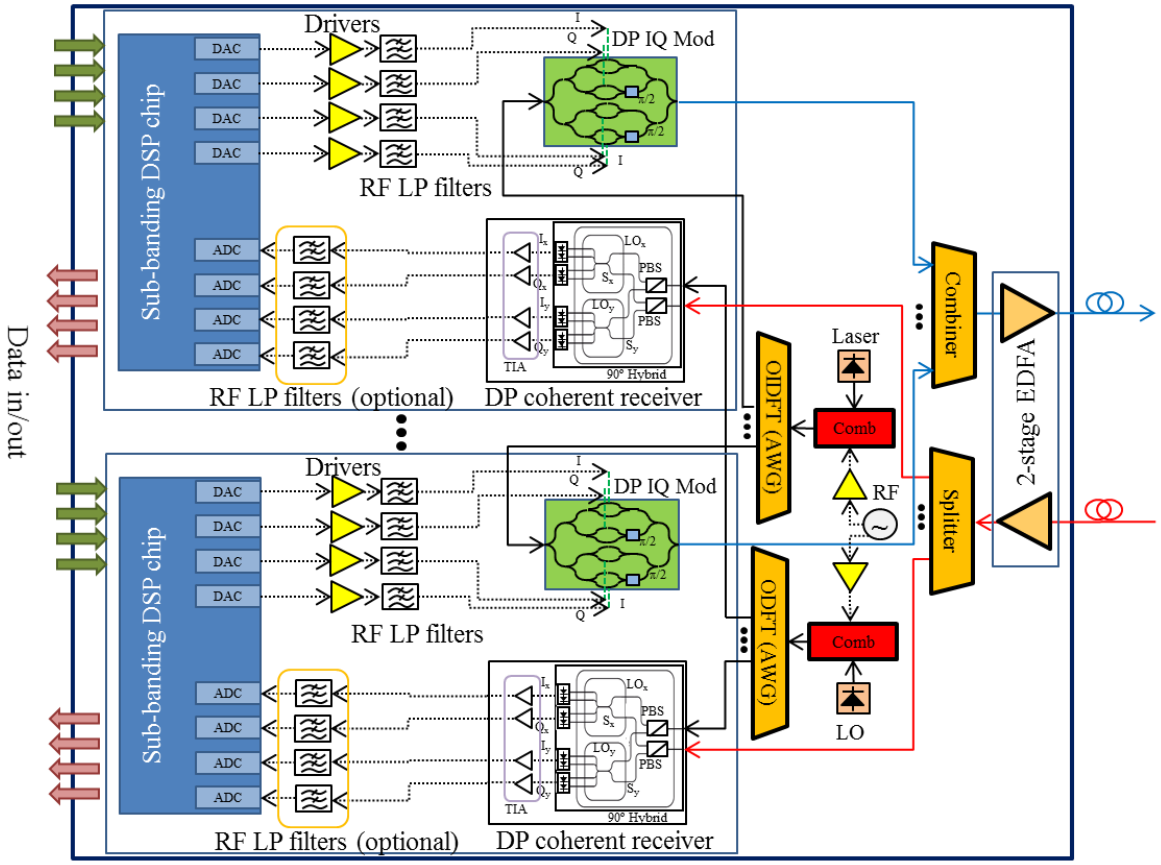


Figure 2.15 Design of an ASTRON OS-OFDM transceiver with a CW laser and a comb generator.

In Table 2.12 we show the cost and power consumption of the OS-OFDM transceiver implementation. The cost was estimated to be the same as that of a super-channel transceiver based on electrical multiplexing schemes (Table 2.6), but the use of sub-banding DSP results in power consumption savings since we have about 1/2 the number of multipliers and also our sampling rate is almost half

that of a conventional receiver (which use twice oversampling, while we can use about 1.1x oversampling). So we almost cut by one quarter the power of the DSP operation (not the FEC), which accounts for half the consumption of a conventional receiver ASIC. So 1/4 of 38.5W (cf. Table 2.1) divided by 2 is 4.8 W. We add 19.25 W to this amount for FEC and other yields, and we obtain ~24 W, which we can conservatively bring up to 30 W. These savings in DSP power consumption lead to a reduction in total super-channel transceiver power of ~18% with respect to the implementation for electrical multiplexing schemes presented in subsection 2.1.2.1. FEC advances may also reduce the other half of the DSP power consumption. For further details, cf. subsection 2.2.3.1.3.

Table 2.12 Relative cost and power consumption of the OS-OFDM super-channel transceiver implementation. (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver.

Component	Relative unit cost (*)	Power (W) [max]	#	Relative cost (*)	Relative cost (**)	Total power (W)
DSP Chip	0.36	30.0	8	2.88	15.04	240.0
PM IQ Mod	0.22	0.0	8	1.04	5.41	0.0
Laser (Tx & Rx LO)	0.05	1.5	2	0.06	0.34	3.0
4-Port Modulator Driver	0.07	6.0	8	0.35	1.80	48.0
RF LP filter	0.00	0.0	64	0.14	0.72	0.0
DP Coherent Receiver	0.22	1.5	8	1.04	5.41	12.0
Variable gain dual-stage amplifier	0.18	12.0	1	0.11	0.56	12.0
Comb generator modulator	0.18	0.0	2	0.22	1.13	0.0
Comb generator mod. driver	0.07	2.0	2	0.09	0.45	4.0
1:N AWG	0.02	0.0	2	0.02	0.11	0.0
				5.93	30.98	319.0

2.2.3 DSP power consumption analysis

To carry out a more thorough analysis of the power consumption of the candidate implementations for the ASTRON project Rx DSP (OS-OFDM and AO-OFDM), let us approach the study from the angle of the ASIC technology and divide it into DSP processes implementing linear and nonlinear equalization techniques.

After evaluating the computational complexity of the eOFDM/NWDM and AO-OFDM DSP algorithms, we focus on the filter-bank approach in the OS-OFDM transceiver implementation. All these DSPs can only compensate for linear impairments. To enhance the DSP's capability to mitigate fibre impairments, we then confine our attention to the following nonlinear equalization techniques:

- digital back-propagation based on split-step Fourier method (DBP-SSF)
- inverse Volterra series transfer function nonlinear equalizer (IVSFT-NLE)

and draw a computational complexity comparison between these two equalization techniques to estimate the power consumption of the corresponding equalization stages based on the ASIC technology.

2.2.3.1 Computation complexity evaluation of linear equalization schemes

This section is devoted to the comparison and discussion of the computational complexity in terms of real time multiplications/additions of three linear-equalisation schemes. First, we evaluate the square-root-raised-cosine (SRRC) and FFT/IFFT computational complexity to enable long-haul eOFDM/NFDM super-channel transmission. It could also be regarded as a lead-in to the calculation of the DSP-block computational complexity for the digital equalization of linear impairments. We then study the transmission performance and computational complexity of the ASTRON AO-OFDM solution, and we provide some power-consumption values assuming a 90-nm ASIC technology. Finally, we estimate the complexity of OS-OFDM systems with filter-bank receiver and gauge it against a conventional receiver solution.

2.2.3.1.1 SRRC and FFT/IFFT computational complexity analysis for eOFDM/NFDM super-channel transceivers

The FFT/IFFT is the DSP block with the major requirement of arithmetic processing units both to implement the digital square-root-raised-cosine (SRRC) filter for NWDM and in the eOFDM transceiver implementation. For FFT, the total number of complex multiplications is in the order of N^2 if we consider an IFFT block with N points. Considering a Cooley-Turkey FFT approach, an N-point, radix-r complex valued FFT consists of $(N/r)\cdot\log_2 N$ "butterflies" operations, where each butterfly consists of a number of (r-1) two-terms complex multiplications and 2(r-1) two-terms complex additions. In general, the standard Cooley-Turkey approach can be optimized considering that some trivial multiplication are present in the algorithm, resulting from the particular values of some twiddle factors. In a real DSP, all the operations are done between real quantities, thus the complex mathematics required by the FFT algorithms must be implemented using real multiplications and sums. Considering a radix-2 and radix-4, the number of operations needed with simplifications are shown in Table 2.13.

By treating the even and odd-numbered samples with the most efficient algorithm each, the split radix FFT (SRFFT) algorithm reaches even better performance than the radix-2 and radix-4 approaches. The resulting algorithms have one of the lowest known number of operations (multiplications plus additions) that are currently implemented in modern FFT techniques, as well as the minimum number of multiplications among practical algorithms.

Table 2.13 Computational complexity for radix-2/4 and split-radix for complex data.

	Real Multipliers #	Real Adders #
Radix-2	$3/2N\log_2 N - 5N + 8$	$7/2N\log_2 N - 5N + 8$
Radix-4	$9/8N\log_2 N – 43N/12 + 16/3$	$25/8N\log_2 N – 43N/12 + 16/3$
Split-radix FFT(Duhamel)	$N\log_2 N – 3N + 4$	$3N\log_2 N – 3N + 4$

In Table 2.14 and Table 2.15 we report the number of real multiplications and sums, respectively, for direct DFT, radix-2, radix-4 and SRFFT.

Table 2.14 Total number of real multiplications per sample for complex data of direct DFT, Cooley-Tukey, Radix-2, Radix-4, and Split-Radix algorithms.

DFT	Direct DFT	Cooley-Tukey FFT	Radix-2 FFT	Radix-4 FFT	Split-radix FFT
2	16	32	1	0	0
4	64	96	0	0	0

8	256	224	4	0	4
16	1024	704	24	20	20
32	4096	1664	88	0	68
64	16384	5376	264	208	196
128	65536	12800	712	0	516
256	262144	41984	1800	1392	1284
512	1048576	100352	4360	0	3076
1024	4194304	331776	10248	7856	7172
2048	16777216	794624	23560	0	16388
4096	67108864	2637824	53256	40624	36868

Table 2.15 Total number of real sums per sample for complex data of direct DFT, Cooley-Tukey, Radix-2, Radix-4 and Split-Radix algorithms.

DFT points	Direct DFT	Cooley-Tukey FFT	Radix-2 FFT	Radix-4 FFT	Split-radix FFT
2	8	4	5	0	4
4	48	24	16	16	16
8	224	64	52	0	52
16	960	256	152	148	148
32	3968	640	408	0	388
64	16128	2304	1032	976	964
128	65024	5632	2504	0	2308
256	261120	19456	5896	5488	5380
512	1046528	47104	13576	0	12292
1024	4190208	159744	30728	28336	27652
2048	16769024	385024	68616	0	61444
4096	67092480	1294336	151560	138928	135172

The implementation of the SRRC finite impulsive response (FIR) filter in FPGAs/ASICs is one of the major sources for the computational complexity. Two different basic approaches are possible for the realization of the filtering function: 1) Time domain and 2) Frequency domain.

Examples of such algorithms are: 1) Time Domain convolution, 2) Time Domain convolution with symmetric/antisymmetric impulse response, 3) Frequency Domain Block convolution (Overlap & Save, Overlap & Add methods), and 4) Look-up Table.

In the convolution with arbitrary FIR digital filter, we have *x(n)* with *length-N* considered to be the input signal, *h(n)* filter coefficients *length-M*, and *y(n)* output with length *N+M-1*. In convolution with an arbitrary impulsive response of *M* taps, we have *M* sum and *M* multiplication for sample, so the total number of operation required is *2M*. For this reason it is convenient to use this algorithm only when the number of the taps is very small.

For filters with a longer impulse response, it is preferable to adopt a FIR filter with symmetric/antisymmetric impulsive response because it halves the number of real multiplications (equal to *M/2*), keeping the number of real additions equal to *M*.

The most common way to achieve "fast convolution" is to realize it in the frequency domain by taking advantage of the efficient FFT/IFFT algorithms. It can be implemented in two forms, Overlap & Add (OA) and Overlap & Save (OS). The input stream x[n] is divided into subsequent blocks of *L* samples, with length of the blocks longer than the impulse response length (taps number). *M* is the number of taps of the filter, and (*M-1)* zero samples are added for circular convolution. In fact, if a length-*M* filter *h(n)* is circularly convolved with a length-*L* x(n), the first $M - 1$ samples are wrapped around and thus

is incorrect. If we truncate the index sample in the interval: $M - 1 \leq n \leq L - 1$, the final convolution is a linear convolution, and the result is correct. We discard first *M − 1* points in each output block and concatenate the remaining points to create y (n) in the case of OS. Alternatively, y(n) can be obtained by overlapping the last *M − 1* samples in the current block with the first *M − 1* samples of the next block by adding the results, in the case of OA. The FFT size *N* is more efficient if it is a power of 2, where $N = L + M - 1 = 2^k$, so the efficiency of the algorithm requires using blocks of the highest possible length compatible with the availability of an efficient FFT.

The computational complexity is evaluated in terms of required (real) multiplications $MR = 4\,(1 + log_2\,N)\,\frac{N}{L}$ or sums per input sample $AR = 2\,(1 + 3\log_2 N)\,\frac{N}{L}$. In Table 2.16 the real operations/sample are shown, where by operation we mean multiplication/sum, for 160 taps SRRC filter with OA implementation and 1024 IFFT points in case of radix-4 and split radix algorithm. In this table, we have chosen radix-4 and split-radix (and have excluded radix-2) because radix-2 requires more real operation than the chosen alternatives in the case of 1024 points IFFT.

Table 2.16 DSP computational complexity cost in number of real operations per sample for complex data in the cases of SRRC FIR filter with 160 taps (first row) and 1024 points IFFT (second and third rows).

	Real Multipliers (operation/sample)	**Real Adders (operation/sample)**
SRRC FIR filter *160 taps*	67	93
Radix-4 IFFT 1024 points	7856	28336
Split-Radix IFFT 1024 points	7172	27652

Given the real operations/sample, we can approximately estimate the real operations/bit for eOFDM & NWDM. In the case of NWDM, the number of samples per symbol $SpS_{SRRC} \leq 2(1+\alpha)$, where α is the spectral roll-off factor of SRRC. The number of operations/bit is estimated by the following formula for both in-phase (I) and quadrature (Q) signal (for this reason in the following formula there is a factor of 2):

$$RO_{SRRC} = 2*SpS*N_{RO/sample}/\log_2(M),$$

with M = 4 order of constellation, and $N_{RO/sample}$ number of real operations per sample.

For eOFDM the estimated formula can be written as:

$$RO_{IFFT} = 2*SpS*\ N_{RO/sample}/\log_2(M)/N_{IFFT},$$

where $SpS_{IFFT} \geq 1$.

The complexity in real operations per bit is given in Table 2.17 for NWDM (first row, obtained by calculating RO_{SRRC} –given by the equation above– with the values for SRRC FIR filter 160 taps shown in Table 2.16) and eOFDM (second and third rows, obtained by calculating RO_{IFFT} –given by the equation above– with the values for radix-4 and split-radix IFFT 1024 points, respectively, shown in Table 2.16).

From Table 2.17 it results that the DSP complexity for SRRC pulse shape implementation with 160 taps is higher than that for eOFDM with 1024 IFFT-size and 20% of virtual subcarriers (~15/6 times more complex in terms of real multiplications/additions). The complexity of SRRC pulse shape can be reduced if multiband filtering or look-up tables (LUT) are used. For instance, we can gain savings in the order of 40% if the integrated circuit allows the optimization of the IFFT algorithms (thus, the

complexity reduces to ~9/4 times). If LUTs are used we can avoid the multiplications and also compensate for the nonlinearity due to the modulators.

Table 2.17 Complexity in number of real operations per bit for complex data in the cases of SRRC filter with 160 taps (first row) and 1024 points IFFT with 20% virtual subcarriers (second and third rows).

	Real Multipliers (operation/bit)	Real Adders (operation/bit)
Overlap & Save FIR SRRC with 160 taps, α = 0.1	146	204
Radix-4 IFFT - Size 1024, 20% virtual subcarriers	10	36
Split-Radix FFT - Size 1024, 20% virtual subcarriers	9	35

We now compare the operation per bit between NWDM and eOFDM for CD compensation. We assume overlap-and-add algorithm for the FIR implementation. The overlap length is found by the following formula: $L = \frac{c \cdot L_{SMF} \cdot D \cdot f_{max} \cdot F_s}{f^2}$, with c speed of light [m/s], L_{SMF} fiber length [km], D dispersion parameter [ps/(nm km)], f_{max} maximum frequency edge of the signal, F_s sampling frequency of ADC, and FFT-size: $N_{FFT-size} = p \cdot L$, where p usually is 2 in the case that the number of receiver sample blocks is equal to the number of overlap lengths. For lower p the algorithm efficiency is increased. The total number of real multiplications per sample for two polarizations, using the split-radix formula, from Table 2.13, for the FFT implementation is: $OM_{sample,PM-QAM} = 4 \cdot M_{split-radix} + 8 \cdot N_{FFT-size} + N_{FFT-size}$, where $M_{split-radix} = N_{FFT-size} \cdot log2(N_{FFT-size}) - 3 \cdot N_{FFT-size} + 4$. The total number of real additions per sample for two polarizations is given by: $OA_{sample,PM-QAM} = 4 \cdot A_{split-radix} + 4 \cdot N_{FFT-size} + N_{FFT-size}$, where $A_{split-radix} = 3 \cdot N_{FFT-size} \cdot log2(N_{FFT-size}) - 3 \cdot N_{FFT-size} + 4$. The number of real operations per bit is given, respectively, for multiplication and addition in the case of NWDM by:

$$OM_{bit,PM-QAM} = \frac{SpS}{log2(M) \cdot (N_{FFT-size} - p \cdot L)} (4 \cdot M_{split-radix} + 8 \cdot N_{FFT-size} + N_{FFT-size})$$

$$OA_{bit,PM-QAM} = \frac{SpS}{log2(M) \cdot (N_{FFT-size} - p \cdot L)} (4 \cdot A_{split-radix} + 4 \cdot N_{FFT-size} + N_{FFT-size})$$

where SpS is the number of samples per symbol.

For eOFDM, following Poggiolini's model [15], we can write the real operations per bit (for multiplication and addition) as:

$$OM_{bit,PM-eOFDM} = \frac{2}{log2(M) \cdot N_{SC'}} \cdot (SpS_{IFFT} \cdot N_{SC'} \cdot log2(SpS_{IFFT} \cdot N_{SC'}) - 3 \cdot SpS_{IFFT} \cdot N_{SC'} + 4) + \frac{4}{log2(M)}$$

$$OA_{bit,PM-eOFDM} = \frac{2}{log2(M) \cdot N_{SC'}} \cdot (3 \cdot N_{SC'} \cdot SpS_{IFFT} log2(SpS_{IFFT} \cdot N_{SC'}) - 3 \cdot SpS_{IFFT} \cdot N_{SC'} + 4) + \frac{2}{log2(M)}$$

where $N_{SC'} = \frac{k^2}{k-1} \cdot 8 \cdot D \cdot L_{SMF} \cdot R^2 / log2(M)^2$ is the increased number of subcarriers to support cyclic prefix while keeping the total data rate R constant, and k is the CD-induced overhead.

Let us choose M = 4, for PM-QPSK modulation, k = 1.2, R = 112Gbit/s, p = 2, SpS = 2 and $SpS_{IFFT} = 1.2$. Figure 2.16(a) shows the number of real additions per bit as a function of the fiber length for only CD compensation, with $OA_{bit,PM-eOFDM}$ having been represented by the red line & $OA_{bit,PM-QAM}$ by the blue line. Figure 2.16(b) shows the number of real multiplications per bit versus the fiber length for eOFDM (blue line) and NWDM (red line) for only CD compensation. In this specific case, the eOFDM shows better performance per bit than NWDM for fiber length higher than 100km. However, as

pointed out by Poggiolini in [15], this difference should not be taken as a decisive decision, but rather other aspects should be taken into account.

The choice between the two architectures is rather complex and also depends on other factors like: power consumption in the case of reduced number of channels, optimized libraries, and receiver complexity.

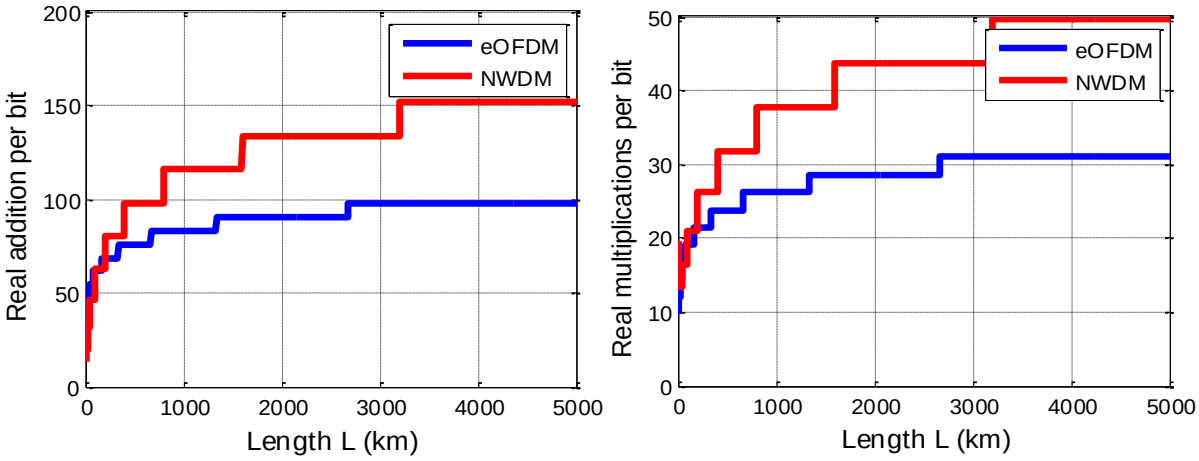


Figure 2.16 Number of (a) real additions and (b) real multiplications per bit versus the fiber length L (m) for eOFDM (blue line) and NWDM (red-line) in the case of CD compensation only.

2.2.3.1.2 *Study of transmission performance and computational complexity of the ASTRON AO-OFDM solution*

To study the transmission performance of the super-channel transceiver implementation described in section 2.2.1.2, we use the following parameters. The optical link is composed of N spans, each including a single mode fibre (SMF) of Lspan = 80 km length and an erbium doped fibre amplifier (EDFA) with NF = 6 dB noise figure, whose gain completely compensates for the span losses. The fibre attenuation is α = 0.2 dB/km, the dispersion parameter D = 17 ps/nm/km, the dispersion slope S = 0.07 ps/nm^2/km, the non-linear parameter $(W\cdot km)^{-1}$ and PMD = 0.1 ps/(km)$^{1/2}$.

We are interested in investigating the sensitivity in terms of required OSNR (ROSNR) as a function of Rx bandwidth in BtB and after 37 span, accounting also for non-linear effects, in the case of two different sampling rates equal to 4*R_s and 6*R_s for PM-QPSK modulation only, due to current ADC sampling rate limitations. We simulated 21 subcarriers PM-QPSK with a laser linewidth of 300 kHz. To compensate for CD a FDE equalizer with a FFT-size equal to 2048 is used. For PMD equalization we use four FIR filters with 13-taps each, and joint FFCPE with 31 symbols window length is used for phase estimation. The results are presented in Figure 2.17.

From Figure 2.17, we observe that by using 4 samples per symbol the ROSNR, after 37 spans, is 12.5 dB and it further increases if the Rx bandwidth becomes greater than 23 GHz. This is a non-trivial result, and shows that the Rx bandwidth must be chosen carefully in order not to have additional OSNR penalty. When 6 samples per symbol are used the ROSNR, after 37 spans, was found to be 11.7 dB for a minimum Rx bandwidth of 25 GHz. Even in this case, when the Rx bandwidth is greater than 37 GHz the ROSNR tends to increase.

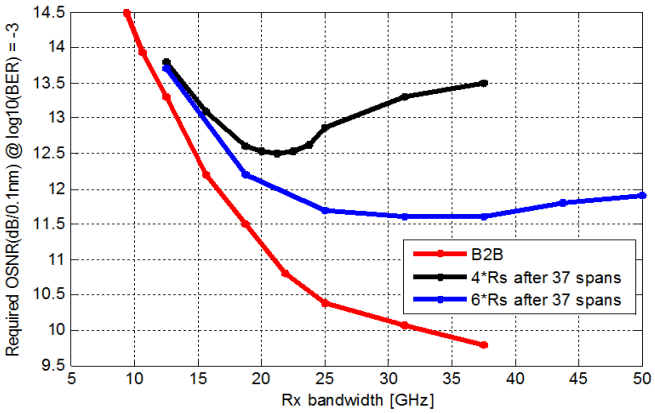


Figure 2.17 ROSNR as a function of the Rx bandwidth in back to back (BtB) shown in red line, after 37 spans for a sampling rate of 4*Rs in black line and 6*Rs in blue line. Rs=12.5Gbaud.

The algorithm for AO-OFDM, as for NWDM, is in principle well known and commonly used offline for experiments or sometimes even used in a real-time FPGA implementations. The main limitation is the computational complexity and power consumption. We used two FDE for CD compensation, one for each polarization, employing the overlap and save block wise algorithm and assuming that the total accumulated CD is known a priori. We divided the received signals in blocks, called FFT-size, with an overlap fixed to half size of the block. We then took the FFT of each block and multiplied it by the inverse fibre transfer function. By taking the IFFT we are able to obtain the transmitted signals. In Figure 2.18 we show the ROSNR at BER of 10^{-3} as a function of the FFT-size after 37 spans of 21 PM-QPSK-modulated AO-OFDM subcarriers, considering also the nonlinear effects, for two different sampling rates, 4*R_s (black line) and 6*R_s (red line).

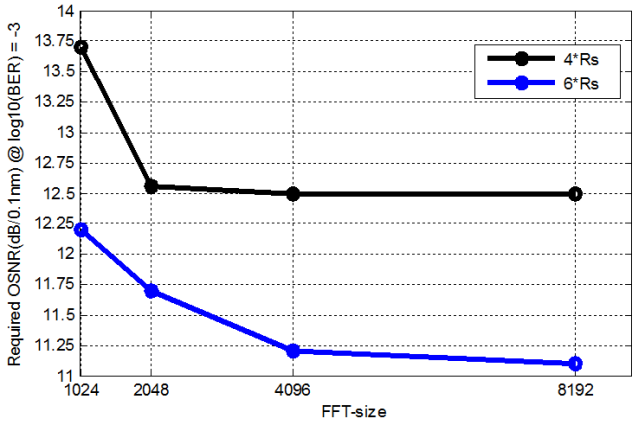


Figure 2.18 ROSNR as a function of FFT-size after 37 spans for a sampling rate equal to 4*Rs (black line) and 6*Rs (blue line).

It is evident from Figure 2.18 that, in the case of using six samples per symbol (corresponding to 75 GSa/s), we obtain better performance in terms of ROSNR. For instance, if FFT-size is equal to 2048 we gain 0.85 dB compared to the case with 4 samples per symbol (50 GSa/s). If we use an FFT-size of 4096 the performance becomes better in the case of 75 GSa/s receiver, but on the other hand the computational complexity also increases. The computational complexity, as the number of real multiplications/additions per bit, with N_{FFT} = 2048 and n_{sc} = 4, is calculated as: a 2048 points FFT needs 32776 real multiplications and 61444 real additions in radix 2 algorithm. In the frequency domain we used 2048 complex taps for chromatic dispersion compensation, equal to 8192 real multiplications and 4096 real additions. After transforming back to time domain, using a 2048 IFFT, we find the total number of operations as 73744 real multiplications and 126984 real additions. At the output of the filter we have 1024 samples T/4 spaced, giving 144.01 real multiplications per bit and 248.03 real additions per bit for a PM-QPSK AO-OFDM signal. Following [16], we find an average energy per bit of

340pJ and power dissipation on an application specific integrated circuit (ASIC) based on 90-nm technology of **17 W** for only CD compensation. For the adaptive equalizer, in time-domain, we can also estimate the power dissipation by measuring the computational complexity in terms of only complex multiplications. We used four FIR filters with 13 taps T/2 spaced each for PMD equalization, giving a maximum of 39 complex multiplications per bit. These complex multiplications require 156 real multiplications and 78 real sums, giving an approximate power dissipation of **13.5 W.**

In addition, for an 8 × 25 Gbaud PM-QPSK super-channel, we estimated the power dissipation for a FFT-size with a length of 1024, for BER = 10^{-3}, in 800 km of SMF, resulting in approximately **304pJ*100Gbit/s = 30 W** for CD compensation per sub-channel. For PMD we used the same complexity as before, with an approximate power dissipation of **27 W** per sub-channel**.** A 100G PM-QPSK conventional receiver, with 256 FFT-size T/2 spaced taps, requires approximately **15 W** power dissipation for only CD compensation. In the case of 8 × 25 Gbaud PM-QPSK AO-OFDM we have twice this power consumption per sub-channel.

However, as pointed out in [17], [18] and [19], and according to values provided by the industry, going from a DSP ASIC manufactured using 90nm/65nm/40nm to the next generation 28nm/20nm CMOS technology results in a power reduction in each process step of approximately 30-40%**.** Therefore, it is envisaged that the power consumption of the ASTRON AO-OFDM DSP (or the transceiver, for that matter, since we estimated the DSP power to be 79% of the total transceiver power in Table 2.11) could approach, to a certain extent, that of a conventional 100G transceiver, due to DSP complexity improvement and more advanced CMOS technologies.

2.2.3.1.3 *DSP complexity of the ASTRON OS-OFDM filter-bank based receiver*

The filter-bank real-time implementation of the receiver as developed under ASTRON exhibits substantial complexity advantage, when implemented over either FPGA or ASIC DSP hardware. Evidently, the full-power savings advantages will be most pronounced in ASIC implementations (as FPGAs have many other power inefficiencies, not related to specific implemented DSP algorithms), but the reduction in the "DSP real-estate" is highly beneficial even for FPGA, having enabled our real-time-DSP-over-FPGA implementation demo for a 16-QAM receiver at 25 or 26.6 Gbaud.

The *complexity rate*, *C*, is defined here as a *complex multipliers complexity rate*: the number of *multipliers per second* (the assumption here is that the multipliers are the heaviest DSP operation, although in certain cases adders contribute non-negligibly). The *complexity figure of merit*, *c=C/R*, we shall display our results in is normalized in terms *multipliers per given standard time interval*, e.g. a symbol interval or a sampling interval or a hardware clock interval, where the rate *R* is the number of standard time intervals per second (we shall representatively use our 1/(419 MHz) FPGA clock interval as the standard clock interval), hence the *complexity rate, C, and complexity figure of merit* , *c* (in short complexity) is equivalently given by the following formulas:

$$C = R\frac{V}{M}\left[\mathrm{m}_{proto\ taps} + \frac{1}{M}\mathrm{m}_{IFFT[M]} + (M-1)\cdot\frac{1}{VN}\mathrm{m}_{FFT[VN]} + (M-1)\cdot\frac{1}{VN}\mathrm{m}_{FFT[N]} + (M-1)\left(m_{IQI} + m_{CFO} + m_{MIMO}\right)\right]$$

$$c(M,N,V) \equiv C/R = V\left[\ p(V) + \frac{1}{M^2}\mathrm{m}_{IFFT[M]} + \frac{M-2}{M}\cdot\left[\frac{1}{VN}\left(\mathrm{m}_{FFT[VN]} + \mathrm{m}_{FFT[N]}\right) + m_{IQI} + m_{CFO} + m_{MIMO}\right]\right];$$

where:

V is the oversampling rate (V=2 in the ASTRON implementation, as the filter-bank is twice under-decimated, i.e. twice oversampled relative to a conventional critically sampled filter bank),

M is the size of the FFT used in the filter-bank (M=16 in ASTRON),

N is the size of the FFT used in the initial per-sub-band filtering of the DFT-spread OFDM sub-band receivers (N=128 in ASTRON for the initial per-sub-band filtering, followed by the DFT-despreader FFT of size N/2=64),

$\mathrm{m}_{FFT[N]} \cong \frac{3}{2} N \log N$ is the complexity per unit sample of a generic FFT of size N (three real multipliers are assumed per complex multiplier) , as per Cooley-Tuckey algorithm,

$\mathrm{m}_{proto\ taps}$ is the number of polyphase taps used in the prototype filter comprised in the filter bank, where $\mathrm{m}_{proto\ taps} = Mp(V); \text{in particular } p(2) = 2 \cdot 2 = 4$ (here p(V) is the number of multipliers per polyphase, M is the number of polyphases – equal to the filter-bank FFT size)

$m_{IQI}, m_{CFO}, m_{MIMO}$ are the respective number of multipliers used in the IQ Imbalance (IQI) correction, the Carrier Frequency Offset (CFO) correction, and MIMO polarization demultiplexing unit in subband receiver ($m_{IQI} = m_{MIMO} = 3 \cdot 2 = 6; m_{CFO} = 3 \cdot 1 = 3$)

The formula above (and various terms therein, separately displayed) is the basis for the evaluation of the filter-bank based complexity solution. For a conventional receiver solution, which is the baseline against which we gauge our complexity comparison, we have assumed a conventional MIMO polarization equalizer with a dozen taps and an Overlap-And-Save (OLS) conventional receiver, modelled as follows (L_s, L_h are the respective duration of the signal record used to perform the OLS FFT and the duration of the overlap window (equal to or exceeding the duration of the impulse response, h) – the other quantities in the formula are self-explanatory). We also optimized over the ratio of $\lambda \equiv L_h / L_s$ in order to "be fair" to the competitive technology (incidentally, such optimization was not published yet to our knowledge).

$$m_{OLS} = m_{FFT[L_s]} + 3L_s + m_{IFFT[L_s]} = L_s \left(\frac{2}{L_s} m_{FFT[L_s]} + 3 \right)$$

$$C_{OLS}(L_s, L_h) = \frac{R}{L_s - L_h} m_{OLS} = R \frac{L_s}{L_s - L_h} \left(\frac{2}{L_s} m_{FFT[L_s]} + 3 \right)$$

$$\lambda \equiv L_h / L_s = overlap\ factor < 1; L_s = L_h / \lambda$$

$$c_{OLS}(\lambda, L_h) \equiv C_{OLS}(L_s, L_h) / R = \frac{1}{1-\lambda} \left(\frac{2}{L_h/\lambda} \frac{3}{2} (L_h / \lambda) \log_2 (L_h / \lambda) + 3 \right)$$

$$c_{OLS}(\lambda, L_h) = 3(1-\lambda)^{-1} \left(\log_2 (L_h / \lambda) + 1 \right)$$

$optimize\ over\ \lambda$:

$$\partial_\lambda c(\lambda, L_h) = \frac{3\lambda(1 + Log[2] + Log[L_h / \lambda]) - 3}{(\lambda - 1)^2 \lambda Log[2]}$$

$$\lambda^{opt}(L_h) = \mathrm{Solve}\left[\partial_\lambda c(\lambda, L_h) = 0, \lambda \right] = \mathrm{Solve}\left[\lambda(1 + Log[2] + Log[L_h / \lambda]) = 1, \lambda \right]$$

$$L_s^{opt}(L_h) = \lambda^{opt}(L_h) \cdot L_h$$

$$c_{OLS}^{opt}(L_h) \equiv c(\lambda^{opt}(L_h), L_h) = 3\left(1 - \lambda^{opt}\right)^{-1} \left(\log_2 \left(L_h / \lambda^{opt} \right) + 1 \right)$$

The comparative complexity is shown in Figure 2.19 below, extracted from our ASTRON disseminated publication [20] (there we just tersely presented the comparison without supplying the analytic details clarifying the calculation, as presented here). The figure caption details the additional parameters and assumptions underlying the comparison.

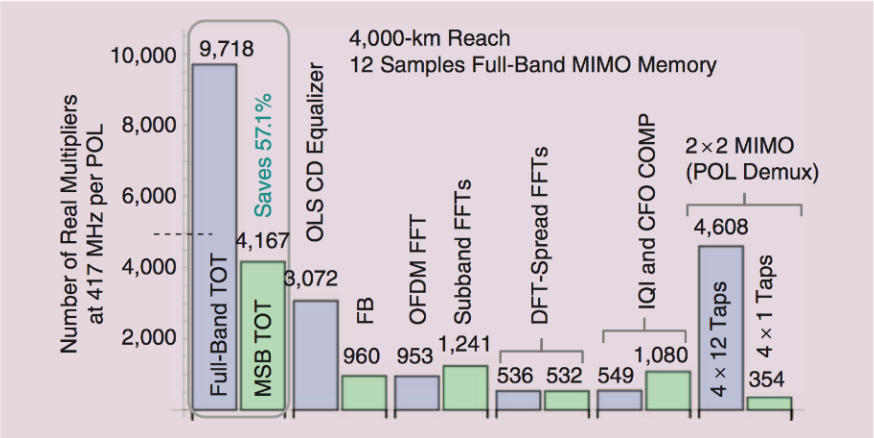


Figure 2.19 The complexity comparison of a full-band conventional Rx versus a multi-sub-band (MSB) DFT-S OFDM Rx for 4,000-km transmission over SMF and for 12 taps of memory for the conventional POL-demux 2×2 MIMO EQZ. Most MSB savings stem from more efficient CD and 2×2 MIMO (PolDemux) EQZ. The 2xUdeci FB "overhead", which enables these savings, is seen to be just several percent of total Rx complexity. Both systems were designed to target the same high spectral efficiency over 2,000-km SSMF: very low CP spectral overhead of 1.56% = 2/128 = 8/1,024. Full-band DFT-S OFDM Tx (used with both Rx-s) uses 1,024-pnt OFDM symbols and inserts eight samples of CP in each of the MSB sub-band Rx-s, simply dropping one CP sample every 128 samples. In contrast, the full-band Rx needs heavy CD and adaptive 2×2 MIMO EQZs in the TD, before the OFDM.

To summarize the complexity comparison, and put it in context, augmenting it by accounting for the extended oversampling rate efficiency afforded by the OFDM + filter-banks approach, let us say the following: as Figure 2.19 indicates, we save 57% of the complexity of the DSP (counting multipliers, i.e. we reduce complexity by a factor of 1/(100%-57%)=1/0.53 = 1.89. In fact, since conventional single carrier-transmission uses twice oversampling and we only oversample by a factor of 1.06, we further reduce computational complexity. This is not to be confused with our twice-oversampling, which occurs within each sub-band (we indeed sample at 1.06 –e.g. 26.6 GS/s for 25 GHz spectrum– and have even demonstrated an RF anti-aliasing filter that allows us to take advantage of the compact spectrum afforded by our DSP, which is the counterpart of tight Nyquist spectrum). Thus, complexity is directly reduced, on account of the substantial reduction in sampling ratio, by another factor of 2/1.06 = 1.89 (in addition to the factor, which also happens to be 1.89, due to the 57% reduction in the DSP complexity). Consequently, altogether, we reduce complexity by a factor of 1.89*1.89 = 3.57.

But, on the negative balance side, the DSP is typically about half the Rx ASIC (the other half is the soft FEC) so we save about a factor of 3.57/2 = 1.79 for the whole Rx digital ASIC. As 1/1.79 = 0.56, then we save 1-0.56 = 0.44 = 44%.

To recap, under the various stated assumptions, an ASIC built according to our ASTRON derived principles, would exhibit 44% complexity savings (weighing in multipliers and sampling rate reductions).

2.2.3.2 Computational complexity evaluation of linear and nonlinear equalization schemes

In this section we draw a comparison between two nonlinear compensators, the IVSTF-NLE and the single/multistep-per-span DBP-SSF equalizer. The 3rd-order IVSTF-NLE discussed in the frame of this deliverable is a simplified version of the work presented in [21], in which accurate Volterra equalizers are derived, and we compare the latter with the single- and three-step per span DBP-SSF only in terms of computational complexity. For brevity, we denote different versions of DBP-SSF equalizers by the abbreviation DBP-SSF$_{Nsteps}$, where N_{steps} is the number of steps per span.

In the absence of polarization mode dispersion (PMD) and polarization-dependent loss (PDL), the Manakov equation describing the evolution of the 2-D vector electromagnetic field envelope in a nonlinear optical fibre is given by [22] and [23]

$$\frac{\partial \mathbf{A}(z,t)}{\partial z}+\frac{a-g(z)}{2}\mathbf{A}(z,t)-\frac{i\beta_2}{2}\frac{\partial^2 \mathbf{A}(z,t)}{\partial t^2}+i\gamma'\left|\mathbf{A}(z,t)\right|^2\mathbf{A}(z,t)=0$$

where $\boldsymbol{A}(z,t)=A_x\hat{x}+A_y\hat{y}$ is the vectorial variable symbolizing the dual-polarization signal, a is attenuation coefficient (km^{-1}), g(z) is the gain coefficient (km^{-1}),

$$\gamma=\frac{2\pi n_2}{\lambda A_{eff}}$$

is the nonlinear coefficient (W^{-1}km^{-1}),

$$\gamma'=\frac{8}{9}\gamma$$

is the effective nonlinear coefficient (W^{-1}km^{-1}), and

$$\beta_2=-\frac{\lambda^2 D}{2\pi c}$$

is the group velocity dispersion (GVD) parameter (ps^{2}km^{-1}).

2.2.3.2.1 *Digital back-propagation based on split-step Fourier method (DBP-SSF)*

In this section we introduce the theoretical model for the digital back-propagation (DBP) technique. DBP refers to a series of algorithms used to compensate the effects of dispersion and fibre nonlinearity. The algorithm calculates the propagation of the signal through the inverse of the actual link, with inverted fibre loss, dispersion and nonlinearity, and negative amplifier gains. It makes use of the efficient and well-known split-step Fourier method. It functions as a zero-forcing equalizer and, although it has been shown to be sub-optimal when the effects of optical noise are included, still provides near-optimal performance at an achievable level of complexity.

The SSF method is implemented using the Manakov equation can be re-written as

$$\frac{\partial \mathbf{A}(z,t)}{\partial z}=\left(\hat{D}+\hat{N}\right)\mathbf{A}(z,t)$$

where $\hat{D}$ and $\hat{N}$ are the linear and nonlinear operators, respectively, defined as follows

$$\hat{D}=-\frac{a-g(z)}{2}+\frac{i\beta_2}{2}\frac{\partial^2}{\partial t^2}$$

$$\hat{N}=-i\gamma'\left|\mathbf{A}(z,t)\right|^2$$

The linear operator accounts for dispersion, loss and gain, and the nonlinear operator accounts for the fibre nonlinear effects. The Manakov equation can be solved numerically by using either the symmetric or the asymmetric SSF method

$$\mathbf{A}(z+h,t)\cong\exp\left(h\hat{D}/2\right)\exp\left(h\hat{N}\right)\exp\left(h\hat{D}/2\right)\mathbf{A}(z,t)\qquad \text{symmetric scheme}$$

$$\mathbf{A}(z+h,t)\cong\exp\left(h\hat{D}\right)\exp\left(h\hat{N}\right)\mathbf{A}(z,t)\qquad \text{asymmetric scheme}$$

where h is the step size [24].

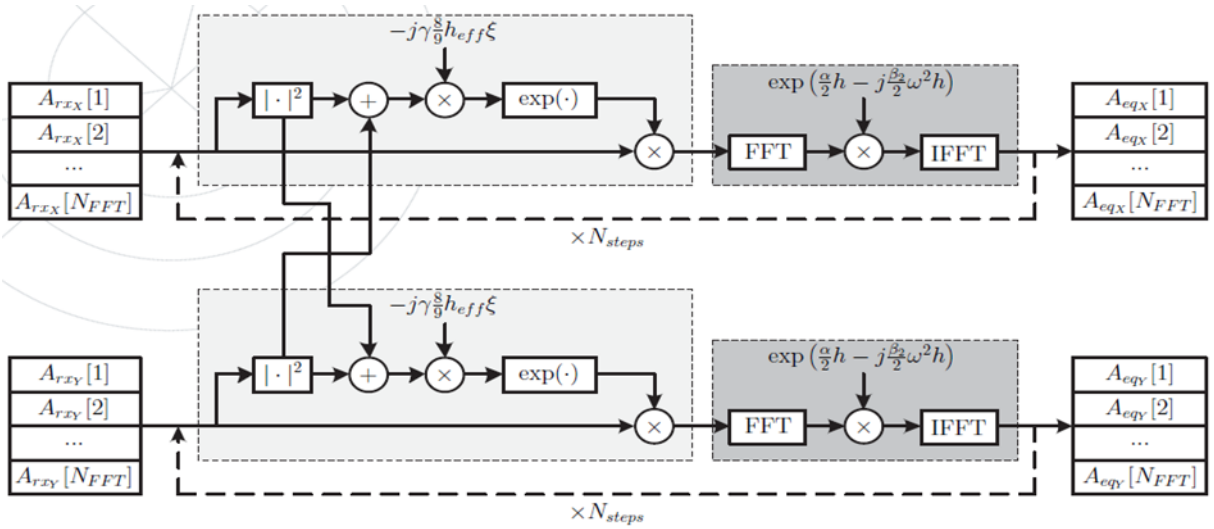


Figure 2.20 Operation principle of DBP-SSF method: A serial model compensating for the nonlinear phase rotations and the linear dispersion by propagating the signal through a fictitious fibre with opposite sign parameters [25].

In the present study, we account for the asymmetric SSF method for the realization of the single-step and three-step per span DBP-SSF. In both cases the equalization process is carried out offline.

The algorithmic steps per span of the DBP-SSF$_{Nsteps}$ method are:

- The nonlinear step:

$$\boldsymbol{A}(z+h,t) = exp(-i\gamma' h|\boldsymbol{A}(z,t)|^2)\boldsymbol{A}(z,t)$$

where $\boldsymbol{A}(z,t)$ is the received signal at the input of the step and it is multiplied by the constant $\gamma' h$ and the total power of x and y polarizations in time domain. This operation is equal to 4 real multiplications per polarization per sample. The operation inside the exponential requires 5 real multiplications per two polarizations per sample.

$$cos\left[\gamma' h\left(A_{x,r}^2 + A_{x,i}^2 + A_{y,r}^2 + A_{y,i}^2\right)\right]$$
$$-isin\left[\gamma' h\left(A_{x,r}^2 + A_{x,i}^2 + A_{y,r}^2 + A_{y,i}^2\right)\right]$$

Thus, we need 4+2.5=6.5 real multiplications per polarization per sample to perform the nonlinear step.

- The linear steps:
  - We take the fast Fourier transform (FFT) per polarization in order to apply the linear compensation part in the frequency domain

$$\boldsymbol{A}(z+h,\omega) = F\{\boldsymbol{A}(z+h,t)\}$$

This operation is equal to $2log_2(N_{FFT})$ real multiplications per polarization per sample, where N_{FFT} is used to denote the FFT block size.

  - Next, we multiply it by the linear transfer function

$$\boldsymbol{A}'(z+h,\omega) = exp\left(-\frac{\alpha - g(z)}{2}h - \frac{i\omega^2\beta_2}{2}\right)\boldsymbol{A}(z+h,\omega)$$

corresponding to 4 real multiplications per polarization per sample.

  - Finally, we take the inverse FFT of the signal per polarization per sample in order to switch back to time domain

$$\boldsymbol{A}(z+h,t) = F^{-1}\{\boldsymbol{A}'(z+h,\omega)\}$$

which requires $2log_2(N_{FFT})$ real multiplications.

Consequently, the total complexity for the DBP-SSF$_{Nsteps}$, in real multiplications, is equal to $(4log_2 N_{FFT} + 10.5) \times N_{steps} \times N_{spans}$, which agrees with the calculation of [21].

2.2.3.2.2 *Design studies on the implementation of real-time digital back-propagation*

Most of the work on digital back-propagation (DBP) reported in the literature is carried out offline because of the DSP complexity (see, e.g. [24]). In this section we present a feasibility study on the implementation of real-time DBP and try to answer the following questions: is it implementable/practical?, and what is the cost in terms of area and power?

DBP is performed in steps along the fibre. Within each step, the effect of dispersion on the signal is compensated in the frequency domain (D^{-1}) followed by compensation of the phase shift induced by the fibre's nonlinearity (N^{-1}), as shown in Figure 2.21(a). Figure 2.21(b) presents a high-level simplification.

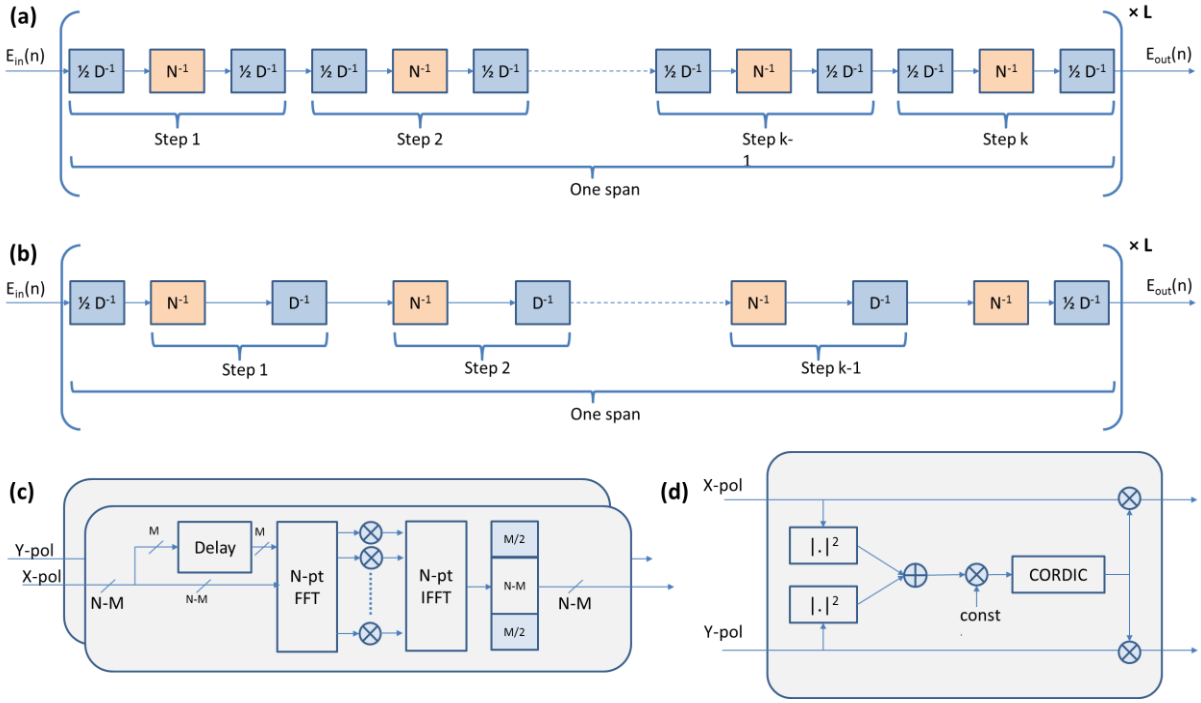


Figure 2.21 Structure of the DBP block. (a) High-level diagram of DBP, in which half the dispersion is compensated (D^{-1}) before the nonlinear compensation within each step. (b) Simplified approach, reducing the number of D^{-1} blocks required. (c) Diagram of the overlap-and-save frequency domain dispersion compensator. (d) Diagram of the CORDIC-based nonlinearity compensator.

Figure 2.21(c) and (d) depict the circuit implementation of DBP sub-blocks. Dispersion compensation is carried out in the frequency domain using the overlap and save method. N-M samples of the received signal are processed in parallel, where N is the size of the inverse fast Fourier transform (IFFT), and M is the overlap size. In the design study described here, an IFFT size of 256 was used, with an overlap size of M=46 samples (note that the overlap size determines the amount of dispersion which can be compensated within each step). The dispersion is compensated using phase shifters on the outputs of the IFFT, following which the signal is transformed back into the time domain using a fast Fourier transform (FFT). M samples at the edges of the FFT window are then discarded. The output of the dispersion compensation block is passed to the nonlinearity compensation block. A value proportional to the signal power is calculated by summing the squared absolute values of the sampled signal in each polarisation. This is then multiplied by a coefficient optimized to obtain the maximum nonlinearity compensation. Since the phase shift to be applied to the signal needs to be converted into Cartesian

format, cartesian-to-polar format conversion is implemented using the CORDIC algorithm, as shown in Figure 2.21(d).

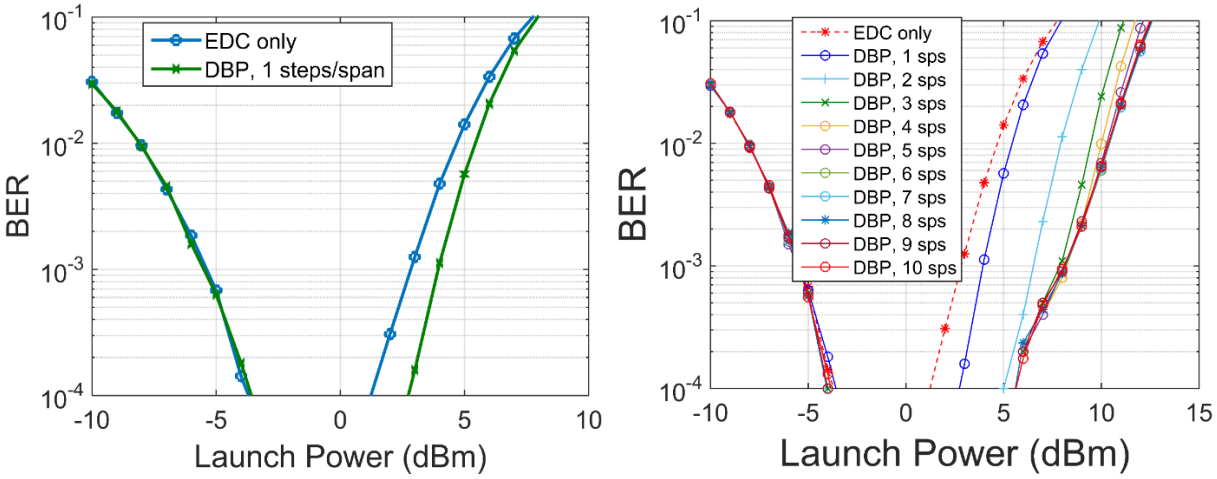


Figure 2.22 Performance of the DBP block. BER versus launch power for 32 Gbaud PDM-16QAM transmission over standard SMF based link of 1200 km, with the number of steps per span (sps) in the DBP algorithm varied.

To assess the performance of DBP, we conducted system simulations and compared electronic dispersion compensation (EDC) vs. DBP with the following system parameters: 32 Gbaud PDM-16QAM, 1200 km standard SMF (SSMF), consisting of 15 spans, each 80 km long; EDFA noise figure = 4.5 dB, and EDC and DBP use 2 samples/symbol. The results of these simulations are shown in Figure 2.22 for 1 step per span (a) and an increasing number of steps per span, from 1 to 10 (b). These plots show the bit error ratio as functions of launch power, with the increasing BER with reducing power (below 0 dBm) being caused by low linear optical signal to noise ratio (OSNR), and BER increasing at higher powers due to fibre nonlinearity. These curves allow us to observe the system performance improvements possible using nonlinearity compensation (compared to electronic dispersion compensation (EDC) only), and to compare the relative gains achievable as the DBP step size is varied. From these simulations, it can be observed that higher steps/span give higher gain, but this trend saturates at 3 steps/span. The maximum launch power at BER = 10^{-3} is increased by approximately 5 dB with 3 steps/span.

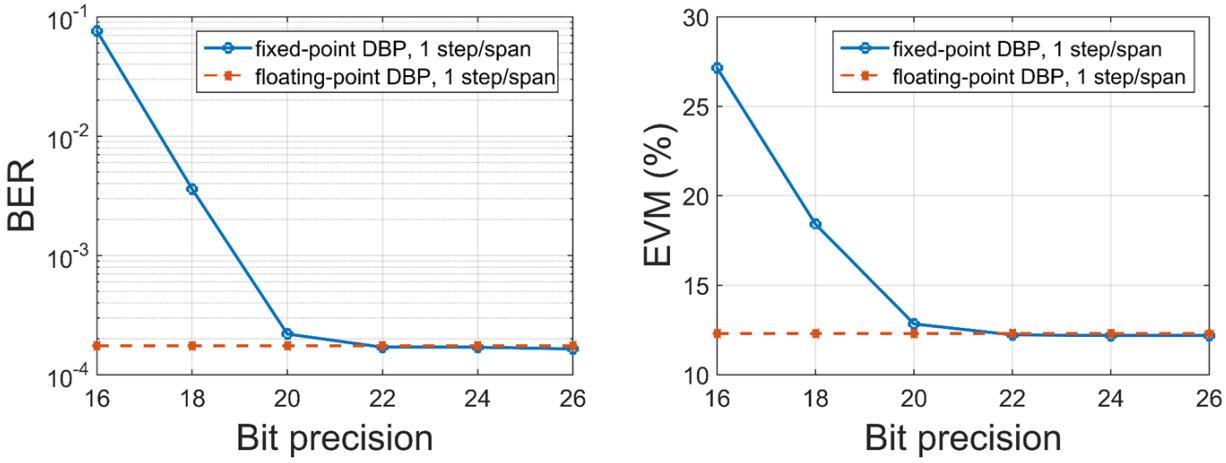


Figure 2.23 Bit width analysis of the DBP circuit considering 1 step per span. The BER and error vector magnitude (EVM) are calculated as functions of the bit precision for the case of 32 Gbaud PDM-16QAM transmission over a standard SMF based link of 1200 km, with one step per span.

The simulations described above used double precision floating point arithmetic to implement the DBP. However, in a practical real-time implementation, lower complexity fixed point arithmetic would

be used. The key question then is, what is the minimum required bit precision (the number of bits used to store and process the signal samples) to avoid additional penalty due to quantisation. Hence, we modelled the DBP circuit in fixed-point representation to determine the minimum required bit precision. The results of this modelling are presented in Figure 2.23, assuming 1 step per span, and Figure 2.24, with 3 steps per span in transmission of 32 Gbaud PDM-16QAM over a standard SMF based link of 1200 km. These results show that, as expected, the greater the number of steps, the more FFTs, which leads to more accumulated error. With 1 step per span, the minimum bit width that could be used without significant penalty was 22 bits. This value increased to 24 bits for the case of 3 steps per span. The explanation for this increase is that, for the greater number of steps, the number of concatenated compensation blocks is greater, and hence leading to greater quantisation errors. Thus, higher resolution is required in each block.

With the minimum bit width in the fixed point implementation of the DBP obtained, the circuit could be designed in detail, and power consumption and required chip area calculated for a given CMOS cell library. This is described in section 2.2.3.2.4.

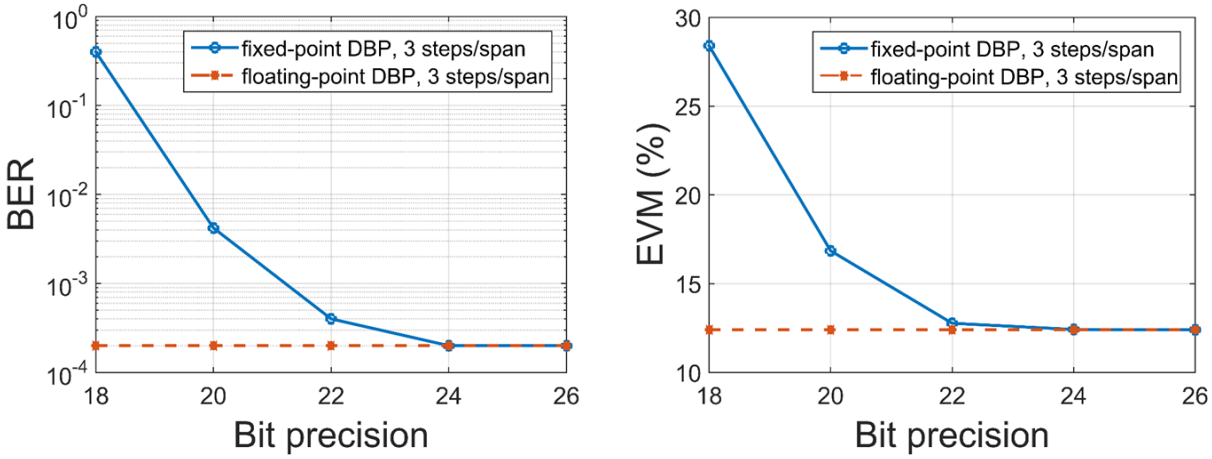


Figure 2.24 Bit width analysis of the DBP circuit considering 3 steps per span. The BER and error vector magnitude (EVM) are calculated as functions of the bit precision for the case of 32 Gbaud PDM-16QAM transmission over a standard SMF based link of 1200 km, with three steps per span.

2.2.3.2.3 *Nonlinear equalizer based on the inverse Volterra series transfer function (IVSTF-NLE)*

In this case the solution of the Manakov equation is an analytical approach using the Volterra series transfer function (VSTF) kernels up to the third order as follows [21]

$$\boldsymbol{A}(\omega,z) = H_1(\omega,z)\boldsymbol{A}(\omega) + \iint_{-\infty}^{\infty} H_3(\omega_1,\omega_2,\omega-\omega_1+\omega_2,z) \times \boldsymbol{A}(\omega_1)\boldsymbol{A}^*(\omega_2)\boldsymbol{A}(\omega-\omega_1+\omega_2)d\omega_1 d\omega_2$$

where

$$H_1(\omega,z) = exp(-\alpha z/2)exp(-i\omega^2\beta_2 z/2)$$

and

$$H_3(\omega_1,\omega_2,\omega-\omega_1+\omega_2,z) = -i\gamma'/4\pi^2 H_1(\omega,z) \times \frac{1-e^{-[\alpha+\beta_2(\omega_1-\omega)(\omega_1-\omega_2)]z}}{a+i\beta_2(\omega_1-\omega)(\omega_1-\omega_2)}$$

are the first- and third-order VSTF kernels, respectively; $\boldsymbol{A}(\omega) = \boldsymbol{A}(\omega,0)$ is the optical signal spectrum at the input of the fibre $(z=0)$, ω is the angular frequency, and ω_1, ω_2 symbolize the discrete frequencies in the sampled spectrum. For the expressions of the IVSTF kernels of the first and third order, we use their simplified versions as they are published in [21]. The simplified versions are based on two assumptions:

1. An optical fibre link with total number of spans N_{spans} without dispersion compensation fibre (DCF). Thus, the IVSTF kernel of the first order is expressed as

$$K_1(\omega) = H_1^{-1}(\omega) = exp\left(i\omega^2\beta_2 N_{spans} L_{span}/2\right),$$

where L_{span} denotes the span length.

2. We take a simplified version of the $H_3(\omega, z)$ in which the second term on the right-hand side is simplified to a term which represents the effective fibre length per span. Also, the waveform distortion within a span is ignored. Under these simplifications, the 3rd-order kernel of the IVSTF is written as

$$K_3(\omega_1, \omega_2, \omega - \omega_1 + \omega_2) \approx \frac{i\gamma^2}{4\pi} \times \frac{1 - e^{-\alpha L}}{\alpha} K_1(\omega) \sum_{k=1}^{N} e^{ik\beta_2 L \Delta\Omega}$$

where $\Delta\Omega = (\omega_1 - \omega)(\omega_1 - \omega_2)$ is the spacing between the discrete frequencies in the sampled spectrum. The detailed derivation of the above expressions can be found in [21].

The equalization process is divided into two parts: The linear part is realized in a single stage for all the fibre spans, whereas the nonlinear part is realized separately for each fibre span. The nonlinear compensation is realized by sweeping the adjustable parameter *c* in the vicinity of its nominal value, $c_0 = -\gamma\left(\frac{1-\exp(-aL_{span})}{a}\right)$. The operation principles of the linear and nonlinear branches of the equalizer are depicted in Figure 2.25 below.

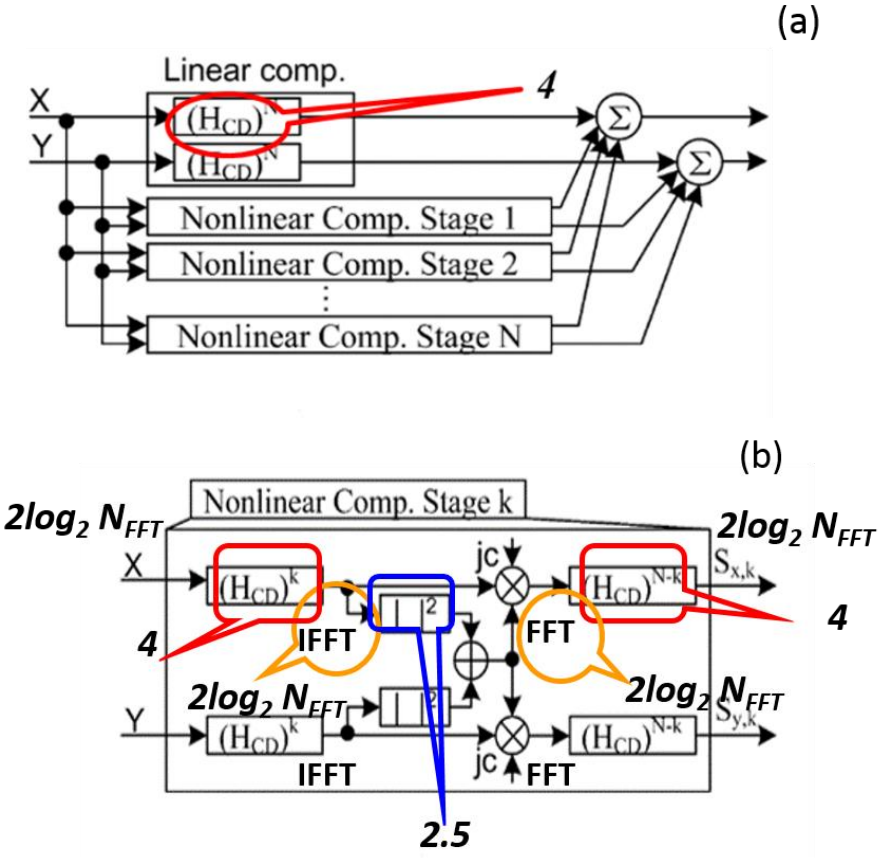


Figure 2.25 Block-diagrams of the 3rd-order IVSTF equalizer. Symbols: $k = 1 \ldots, N_{spans}$ and jc is the nonlinear compensator operating on the time domain. The linear and nonlinear part of the equalizer are depicted in (a) and (b), respectively [21].

In Figure 2.25(a) we present the linear part of the nonlinear equalizer, whose operation is summarized by the following relation

$$S_0(\omega) = H_{CD}^N(\omega)A(\omega)$$

where $S_0(\omega)$ is the output from the linear branch and $H_{CD}^N(\omega) = \left(K_1(\omega)\right)^N$, where $N = N_{spans}$. For this branch of the equalizer only 4 real multiplications per polarization per sample are required.

Figure 2.25(b) depicts one of the *k*th stages of the nonlinear compensator, where $k = 1, \dots N_{spans}$. The necessary number of real multiplications is $10.5 + 4log_2N_{FFT}$ per polarization per sample per nonlinear branch. More specifically, 4 real multiplications are needed for the CD compensation, $4log_2N_{FFT}$ multiplications for the FFT and IFFT, and 2.5 real multiplications for the nonlinear phase computation per polarization per sample. There are 4 more real multiplications at the end of each of the nonlinear branch compensating for the residual chromatic dispersion (CD). For all the branches, $4log_2N_{FFT}$ real multiplications are needed for the FFT and IFFT at the input and at the output of the equalizer. Hence, the total number of real multiplications per polarization per sample is $N_{spans} \times (4log_2N_{FFT} + 10.5) + 4log_2N_{FFT} + 4$.

Finally, the DBP-SSF$_{Nsteps}$ and IVSTF-NLE equalizers are compared in terms of computational complexity (i.e. number of real multiplications) by defining the excess factor in real multiplications as the ratio of the number of real multiplications per polarization per sample required for each equalizer to the number of real multiplications per polarization per sample required for the IVSTF-NLE when using FFT block size equal to 128. The calculations have been made with oversampling ratio equal to 1. In Figure 2.26 we have plotted the excess factor as a function of the FFT block size for the DBP-SSF$_1$, the DBP-SSF$_3$ and the IVSTF-NLE equalizers for 10 spans. We can see that DBP-SSF$_1$ and IVSTF-NLE equalizers differ only slightly in complexity, while DBP-SSF$_3$ appears to be almost three times more complex compared to the previous two.

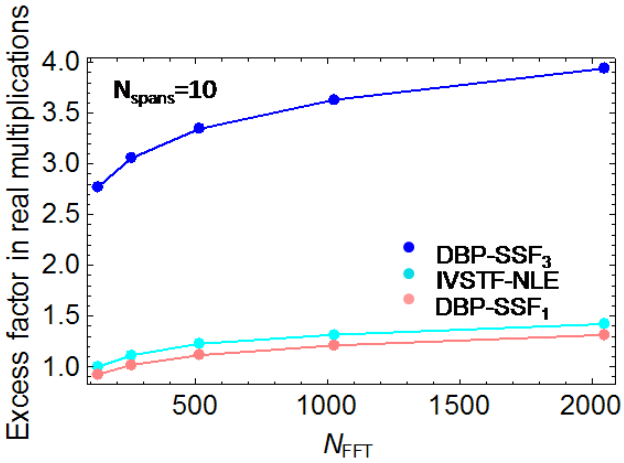


Figure 2.26 Excess factor in real multiplications per polarization per sample vs. the FFT block size (NFFT) when applying the IVSTF-NLE, the DBP-SSF$_1$ and the DBP-SSF$_3$ equalizers after 10×100 km of SSMF.

2.2.3.2.4 *Power consumption analysis based on ASIC technologies*

In this section, we assess, both in real-time and via calculations, the power consumed for the nonlinear compensation when using the IVSTF-NLE, the DBP-SSF$_1$ and the DBP-SSF$_3$ equalizers in a 32 Gbaud PDM-16QAM sub-channel, as described in subsection 2.2.3.2.2. The power consumption of the IVSTF-NLE is estimated only theoretically. In both cases, a 45nm ASIC technology is considered. For precision, we should emphasize that the calculation of the power consumption due to the nonlinear equalizers is a complementary study mostly focusing on the comparison between the power consumption of the analytical nonlinear equalizer IVSTF-NLE compared to the numerical compensation method of the DBP-SSF$_{Nsteps}$. The comparison results, as depicted in Figure 2.27(a) and (b), are provided essentially as an insight rather than an exact estimation.

For the calculation of the power consumption, we have followed the rationale described in [16]. Having calculated the number of real multiplications for the three different equalizers in 2.2.3.2.2, we try to estimate the corresponding consumed power for each one of them. In the case of the IVSTF-NLE, the number of real multiplications, required for its realization, is estimated as follows: the length of the 32 Gbaud PM-16QAM OFDM signal, right before the input of the IVSTF-NLE and after being downsampled to its initial sampling frequency (the one that it had before being oversampled for the transmission), is N=137546 and it is equal to the sum of the number of OFDM symbols in the frame, the number of training symbols used for the channel estimation, the total number of subcarriers (data, null and pilot subcarriers) and the number of samples used for the cyclic prefix. Then, using the aforementioned formula calculating the number of real multipliations per polarization per sample, $Nspans \times (4log_2N + 10.5) + 4log_2N + 4$, for $N = 137456$ and $Nspans = 10$, it gives 860.0189 real multiplications. If we apply the method overlap and save with FFT block size 256 and overlap size of 46 samples, then 184 bits are carried for 32 Gbaud PDM-16QAM. In that case, the number of real multiplications per bit is 4.6740. The number of real multiplications per bit is multiplied by the power per multiplier. The power per multiplier is provided by UCL in the frame of their recent work. Based on this, we calculated that the power consumption for the IVSTF-NLE at 1000 km is 209.482 W. Similarly, we calculated the power consumption of the DBP-SSF_1 and the DBP-SSF_3 equalizers at 1000 km yielding 188.305 W and 618.625 W, respectively. We observed that the power consumption of the IVSTF-NLE is ~21.770 W higher compared to the DBP-SSF_1 equalizer. In Figure 2.27 we show the power consumption of IVSTF-NLE, DBP-SSF_1, DBP-SSF_3 and a linear equaliser for transmission distances ranging from 100 to 1200km.

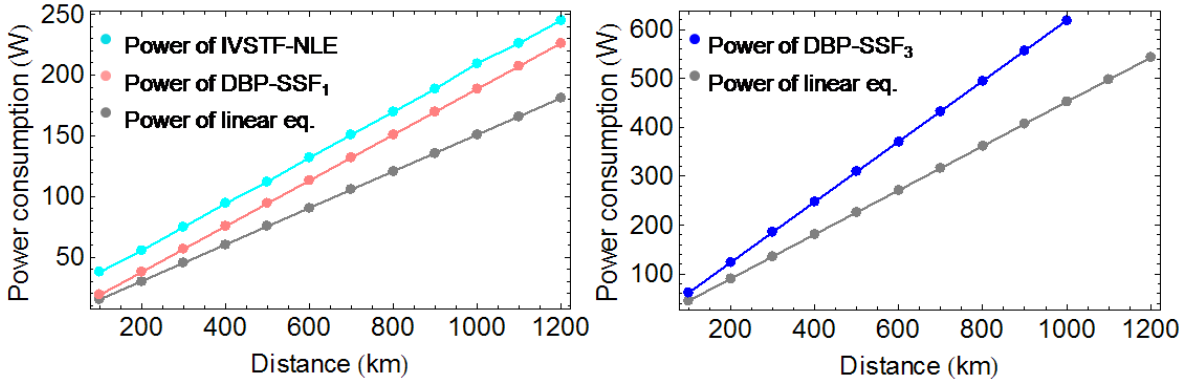


Figure 2.27 Power consumption as a function of the transmission distance for the IVSTF-NLE, the DBP-SSF_1 and the DBP-SSF3 equalizers

For the real-time digital back-propagation circuit, using the minimum required bit width calculated as described in the previous section, and indicated in Figure 2.23 (22 bits for 1 step/span) and Figure 2.24 (24 bits for 3 steps/span) we designed and synthesised circuit components targeting a 45 nm standard cell library. The clock frequency was 305 MHz (throughput of 64 GS/s). With these parameters, we calculated the area and power and compared them with those for an Intel 18-core Xeon processor as an example. We show the results in Figure 2.28 and Figure 2.29.

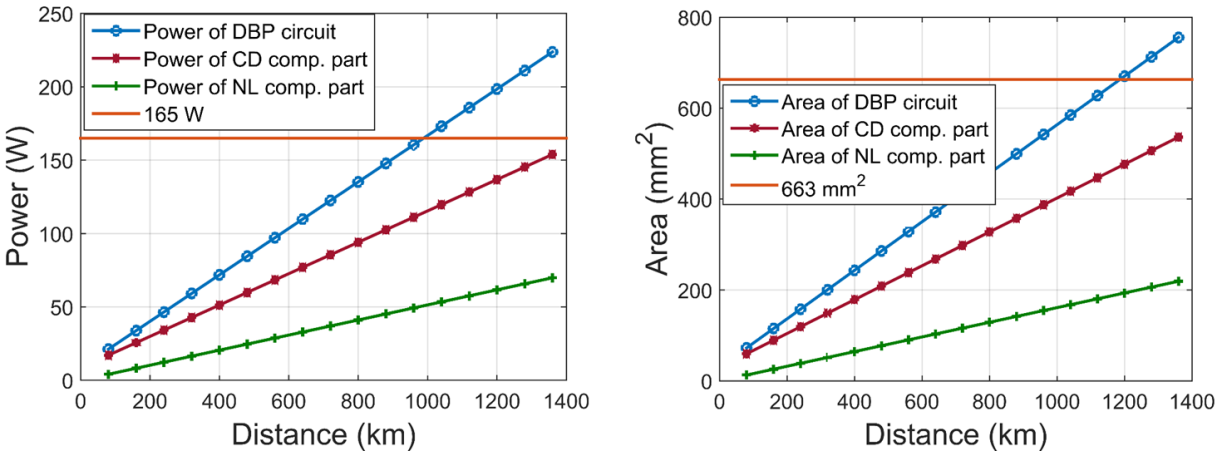


Figure 2.28 Power and area of a DBP circuit assuming 1 step per span. The orange line shows the power and area for an Intel 18-core Xeon processor.

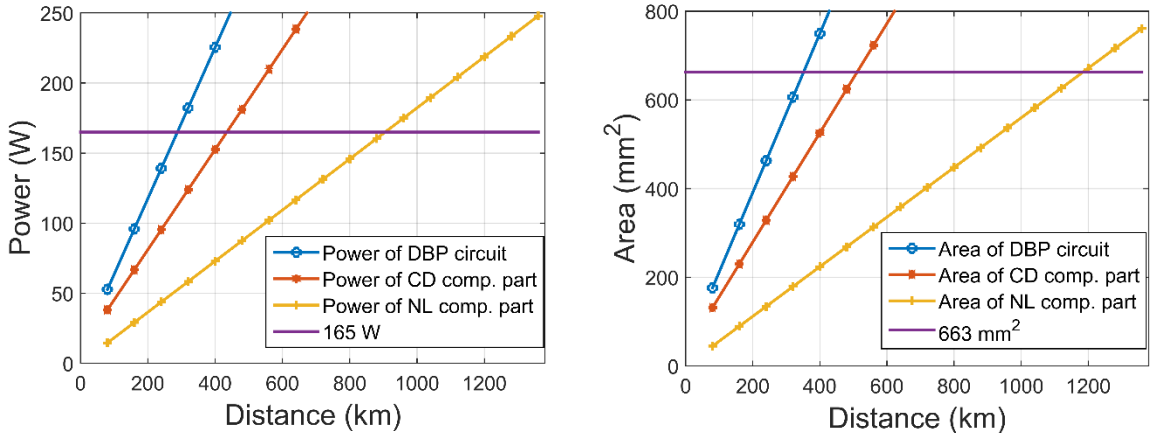


Figure 2.29 Power and area of a DBP circuit assuming 3 steps per span. The orange line shows the power and area for an Intel 18-core Xeon processor.

For 1 step per span, the calculated power consumption reaches 165 W for a 1000 km transmission system, while the ASIC chip area is below 600 mm^2. While these values are high, they are within practically achievable limits, as shown by comparison with the commercially available Intel 18-core Xeon processor chip. The power consumption and chip area for 3 steps per span are more than three times higher, so that, while the performance gains from DBP with this step size is greater, its use is limited to a distance 300 km to remain within the 165W/663 mm^2 limits.

The explanation for the large difference between the power required for CD compensation calculated in section 2.2.3.1.2, and the power for the digital back-propagation design, as shown in Figure 2.27, Figure 2.28 and Figure 2.29, is as follows: for the linear CD compensation carried out in section 2.2.3.1.2 just a single FFT/IFFT pair is required. In the case of the digital back-propagation nonlinearity compensation, the dispersion compensation is carried out in small sections, corresponding to the steps of the split-step Fourier algorithm. For example, for 800 km transmission with 80km step size, this requires 10 separate CD compensators, each with an associated FFT/IFFT pair. Since the majority of the power is used for the FFT/IFFT in frequency domain equalisation, the CD compensation in digital back-propagation is far higher than in linear CD compensation carried out in a single step.

These results were obtained without intensive optimization and can be reduced in a number of ways. Firstly, optimizing the circuit at the algorithmic level by reducing the total required number of steps and using filtered DBP, for example, can lead to significant savings. Secondly, optimization at the implementation level can also yield further reduction in cost. This can be done by using a lower bit

width in the nonlinearity part for example or by using lower CMOS transistor size. The results presented here were based on a 45-nm standard cell library. Using a CMOS technology node with smaller feature size would give a reduction in area and power. For example, the modelling technique in [19] suggests that moving from 45-nm to 22-nm would result in area and power reductions of approximately 3 and 2.5, respectively. All in all, real-time DBP is practical and within the area and power envelope of current high performance chips.

Finally, a recently published work [28] provides an insight on the relative complexity of blocks in a transceiver that works at 100 Gbps using QPSK modulation or at 200 Gbps using 16-QAM. The measure of complexity is power dissipation. The results of this study are summarized in Table 2.18.

Table 2.18 Relative complexity of blocks in a transceiver that works at 100Gbps using DP-QPSK or 200Gbps using 16QAM [28].

Block	100Gb/s QPSK	200Gb/s 16-QAM
FEC Encoder	0.02	0.04
TX DSP	0.02	0.02
BCD Equalizer	0.21	0.21
FFE	0.14	0.14
Carrier Recovery	0.02	0.02
Soft Decision Comp.	0.03	0.03
FEC Decoder	0.22	0.45
Framer/Mapper	0.03	0.06
Miscellaneous	0.14	0.14
AFE	0.17	0.19
Total	1.00	1.30

2.2.3.3 Discussion

The considerations of computational complexity and power consumption of linear and nonlinear equalization schemes were the main focus of section 2.2.3. Firstly, we demonstrated that the DSP complexity for NWDM is higher than that for eOFDM, even though the SRRC-pulse-shaping complexity can be reduced in the region of 40% if multiband filtering or LUTs are used. In fact, a number of experimental studies have shown that NWDM can have a similar or better performance than eOFDM with lower or similar processing complexity [29][30].

Next, the ASTRON AO-OFDM and OS-OFDM receivers were compared with a full-band conventional receiver in terms of computational complexity. It was shown that OS-OFDM can provide 44% savings in complexity for the whole Rx ASIC, whereas in the case of AO-OFDM the complexity for CD compensation (which is, after the SD-FEC decoder, the major contributor to the ASIC power [18]) increases by a factor of 2. These power dissipation values can be reduced by using more advanced CMOS technologies. Going from a 40nm to a 16nm process size would allow bringing the power down by ~50-65%, which combined with the savings brought about by the filter-bank approach, could enable energy savings in the region of 75-85%. This would make it possible for an integrated super-channel transceiver to reduce its power consumption to that of a 100G long-haul line card –including OIF MSA module based on the 40nm CMOS technology, OUT framer and client modules (~150W)–.

Finally, the computational complexity of the DBP-SSF_1, the DBP-SSF_3 and the IVSTF-NLE equalizers was assessed and compared, and we showed that the IVSTF-NLE and the DBP-SSF_1 have almost the same computational complexity, with the latter being only slightly less complex. However, the IVSTF-NLE seems to be almost three times less complex compared to the DBP-SSF_3 equalizer. Finally, the power consumption and the chip area for the DBP-SSF_1 and DBP-SSF_3 based on a 45-nm standard cell library were experimentally estimated. It was shown that the real-time implementation of the DBP-SSF_1 equalizer is within practical limits. On the contrary, the power consumption and chip area of the DBP-SSF_3 are prohibitively high, almost three times higher than those for the IVSTF-NLE, rendering the

implementation of DBP-SSF_3 impractical in real-time systems. Additionally, the power consumption of the IVSTF-NLE, the DBP-SSF_1 and the DBP-SSF_3 was theoretically estimated. The IVSTF-NLE consumes ~21.2W more compared to the DBP-SSF_1 equalizer after 1000 km of transmission distance. A future work targeting the experimental estimation of the IVSTF-NLE power consumption will complete the theoretical results.

2.2.4 Co-packaging and integration

The photonic integrated circuits market is growing at a phenomenal rate as it provides significant improvements in system size, power consumption (e.g. it reduces cooling requirements), reliability and cost [31]. Many factors can affect the projected costs of a new technology, among which the scale (e.g. annual production volume), the manufacturing location (e.g. the difference between producing in the USA and East Asia) and the production yields achievable for each technology have the largest cost implications. The development of the silicon photonics technology has helped in large-scale manufacturing of PICs at low cost. However, InP platforms can, depending on yields, have production costs equal to or lower than silicon photonics for the production volumes expected for telecom and data-centre applications [33]. Table 2.19 summarises the pros and cons of InP and silicon photonics for PIC manufacturing.

Table 2.19 Comparison of InP and silicon photonics technologies [32].

InP	Si
Expensive material	Cheap material
• In is scarce	• 27% mass Earth's crust is Si
Medium yield	High yield
• W.g. material from epitaxy	• W.g. material from original boule
Small footprint	Extremely small footprint
• High index contrast in 1D	• High index contrast in 2D
Native laser	No native laser
Poor native oxide	Excellent native oxide
Low dark current	Medium dark current
Small wafers (75 mm typ.)	Large wafers (300 mm typ.)
• 75 mm typical	• 300 mm typical
• Brittle material	• Strong material
Modulator temperature sensitive	Modulator temperature insensitive
• Band edge moves with temperature	• Carrier density not v. temp. dep.

Daryl Inniss (Ovum) and Vladimir Kozlovat (LightCounting) confirmed at ECOC 2015 Market Focus on Silicon Photonics that InP could have production costs equal to or lower than silicon photonics. Daryl Inniss claimed that no tangible advantage of silicon photonics vs. other integration platforms is foreseen at 100G since volumes fragmentation does not help to reap the CMOS economies of scale. He also said that silicon photonics might play a bigger role in the next cycle (400G). Silicon photonics has been chosen when a low cost module had to be developed from scratch not leveraging on in-house alternative technology (as was the case for the 100G Metro by Acacia). Along the same lines, Vladimir Kozlovat stated that the trigger point for integrated optics to make sense is a function of complexity and targeted volumes. Large volumes alone are not a sufficient trigger. The highest volumes of optical modules shipped nowadays are assembled with discrete devices (FTTx, 100M units). This is expanded upon by Christopher R. Doerr (Acacia) in [32], who explains, for instance, that in low cost, short reach, high-volume applications, there is strong competition from cheap lasers, which puts silicon photonics at a disadvantage, since, as shown in Table 2.19, it has no easy way to integrate lasers. The complexity of beyond 100G transceivers would satisfy the silicon-photonics complexity requirements provided reasonable volumes.

Photonic integration strategies can be divided into three main categories, each of them having its own pros and cons:

- **Hybrid integration (co-packaging):** Devices of different functionalities are assembled and coupled to one another by electrical and/or optical interconnections and packaged into a common module. Required alignment tolerances as well as the combination of different material platforms – having different optical, mechanical and thermal characteristics – are the main challenges of this approach. Meanwhile, monolithic integrated photonic integrated circuits (PICs) are important building blocks in this approach to achieve economic production of compact and high performance modules.
- **Monolithic integration:** Various optically active and passive functions/devices are fabricated on a common semiconductor substrate (e.g. InP) by utilizing a suitable semiconductor material system (e.g. GaInAsP, GaInAlAs). Silicon (Si) is another material system, which has become increasingly important in recent years for photonic integrated circuit fabrication (Si-photonics). The monolithic approach offers a number of potential advantages in terms of footprint (compactness), electrical and optical connectivity between different functional devices, packaging effort, performance (e.g. RF bandwidth), power consumption, robustness, and reliability. Today's InP integration technology allows for reliable and cost-effective mass production of various photonic devices for 1310/1550nm telecom applications by using standard semiconductor manufacturing processes. Moreover, photonic ICs are often used as core pieces in more complex but compact hybrid components to reduce production cost and to improve performance characteristics.
- **Heterogeneous integration**: This relatively new technology [34] can be seen as a specific kind of monolithic approach to integrate two or more semiconductor material systems on a common semiconductor substrate. For example, GaInAsP/InP material is locally placed on a common Si substrate by selective area growth or wafer bonding. The latter is most advanced at present and already proven for first device production. This integration concept benefits from the advantages of both material systems. The GaInAsP system for example is preferably used to provide active photonic functions (e.g. lasing, amplification, detection), while silica or silicon nitride based layers on Si enable optically passive functions of better performance. Last but not least, this technology provides the option to integrate also various electronic functions (combination with monolithic Si electronics)

Notwithstanding the various technological and performance advantages of these integration approaches, the manufacturing cost is a very important economic factor. Reasonable cost savings can be expected by an appropriate combination of hybrid and monolithic integration concepts, by applying exclusively the monolithic approach, or even by using heterogeneous integration in future. The first two concepts mentioned before are investigated in the ASTRON project to develop –for the first time– complex super-channel OFDM/Nyquist-WDM transmitters (Tx) and receivers (Rx), both relying on an integrated AWG as the key element for super-channel multiplexing/demultiplexing. Thus the expected cost for monolithic and hybrid integration are roughly estimated and discussed in the following subsections.

2.2.4.1 Chip integration

In ASTRON, all active sub-elements of the super-channel Tx and Rx are fabricated by using monolithic integration on InP (balanced photodiodes with integrated spherical lens, 4(8)-channel IQ modulator PICs, and entire AO/OS-OFDM Tx PICs (cf. Figure 2.30)). Because the active Tx PICs represent the most challenging components in the project, and thus the dominant cost item at present, the following cost discussion is concentrated on this topic.

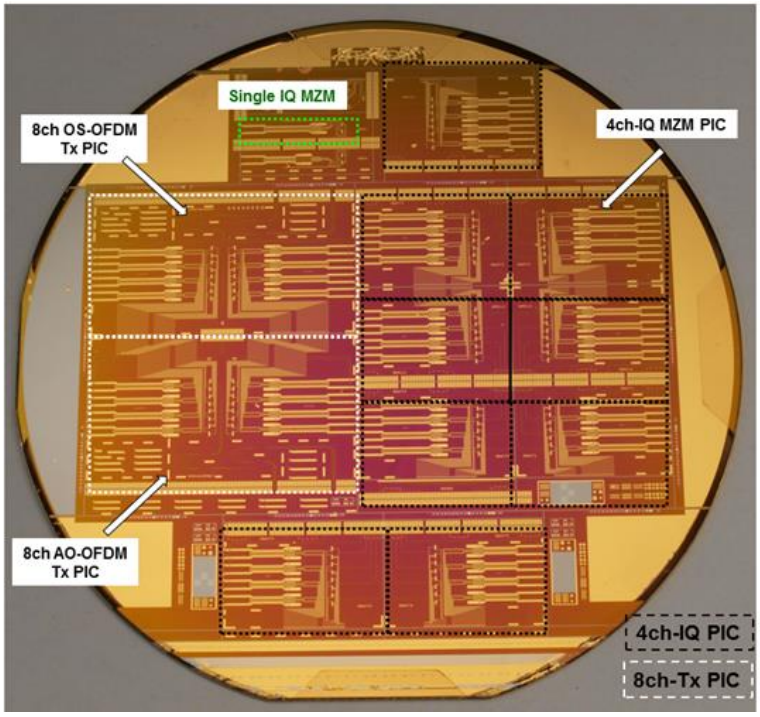


Figure 2.30 Photograph of nine 4ch-IQ (Quad) PICs (or four 8ch-IQ PICs), two 8ch-Tx PICs (AO- and OS-type), and single IQ MZ modulators; all fabricated on a 3-inch InP wafer. The 4(8)ch-IQ PICs are specifically designed for hybrid assembly into the ASTRON 8ch-OFDM transmitter components. The PIC footprints are 2.5 × 12 mm² for a single IQ modulator, 10.5 × 16 mm² for a 4ch-IQ, 10.5 × 32 mm² for an 8ch-IQ, and 16.5 × 28 mm² for the entire Tx PIC.

Figure 2.30 shows a 3-inch InP wafer which was fabricated recently in work package WP3. The wafer integrates 4(8)-channel IQ MZM PICs for hybrid Tx assembly, and – for the very first time – fully integrated monolithic 8-channel OFDM transmitter PICs. All PICs consist of HHI's capacitive-loaded travelling wave electrode (TWE) Mach-Zehnder (MZ) modulators as active building blocks. The different PIC sizes can give us a rough idea of the achievable PIC densities on a 3-inch InP wafer when the number of integrated IQ modulators – i.e. OFDM channels – increases. For comparison, a single IQ MZ modulator is shown in the top left-hand corner of the wafer in Figure 2.30.

The simple relation between achievable number of PICs per wafer and PIC size is shown in Figure 2.31 for available 3-inch and 4-inch InP substrates (cf. black graphs and y-axis on the left). Note that the data are shown on a logarithmic scale. The calculated numbers apply simply to the PIC size and do not make any distinction between different PIC functions. The current PIC sizes of the particular N-channel PICs fabricated in the ASTRON project are depicted by the vertical lines in Figure 2.31.

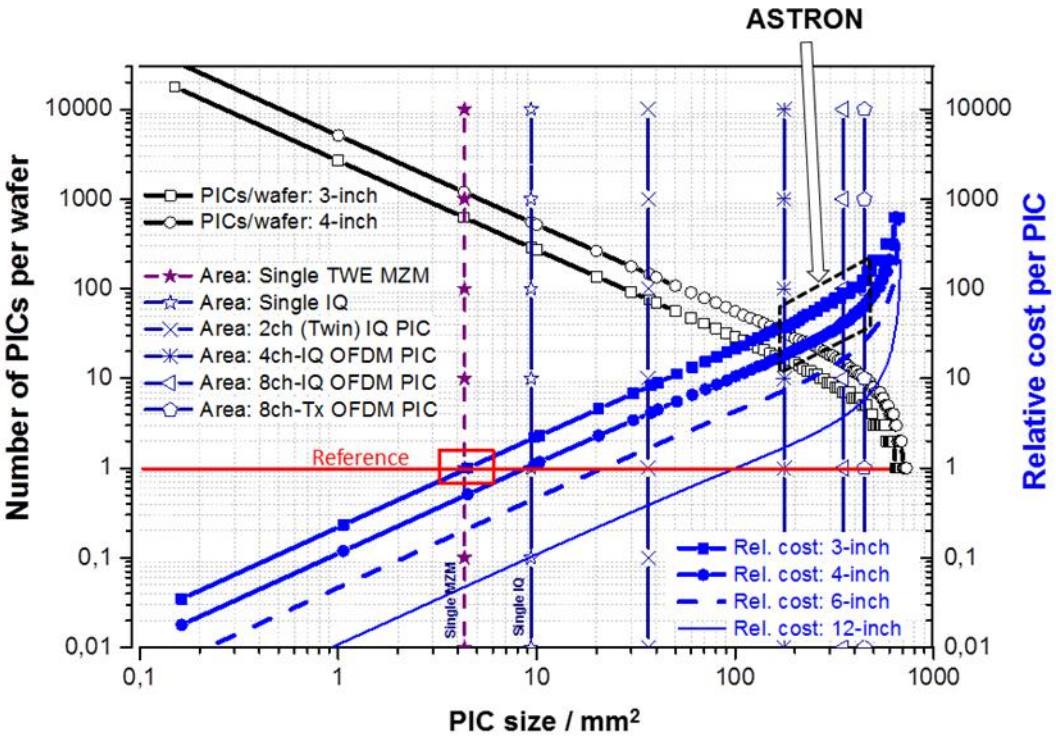


Figure 2.31 Number of PICs per wafer (black data and left-hand y-axis) and relative cost per PIC (blue data and right-hand y-axis) as a function of PIC size and substrate diameter as parameter (PIC yield: 100%, cost reference: single MZ modulator = 1). The vertical lines depict the different N-channel IQ PIC sizes currently fabricated in ASTRON.

It is obvious that the decreasing number of available PICs per wafer with increasing PIC size is accompanied by increasing manufacturing cost. This is clearly depicted by the blue graphs in Figure 2.31 (right-hand axis) showing the increasing relative cost with decreasing number of PICs per wafer for different substrate sizes (assuming 100% on-wafer yield). The cost calculation refers to a single MZ modulator fabricated on a 3-inch InP wafer as a reference (on-wafer cost of a single MZM = 1). Even by considering 100% on-wafer yield, the 2ch-IQ PIC will cost ≈ 8x more than a single reference MZM modulator, the 4ch-IQ PIC ≈ 40x, the 8ch-IQ PIC ≈ 90x, and the fully integrated 8ch-Tx PIC even 110x more (all PICs fabricated on 3-inch wafer, Figure 2.31). This cost increase, simply given by increasing the chip size, will be reduced by a factor of ≈ 2 if a 4-inch InP substrate is used, and even more with larger substrate sizes.

In order to achieve a deeper understanding, the relationship between the number of integrated IQ modulators (equal to the number of OFDM channels) and the resulting PIC footprints is shown in Figure 2.32 (NIQ-PIC: PIC with N integrated IQ modulators, NIQ: Number of integrated IQs (OFDM channels), N=0.5: Single MZ modulator = 0.5IQ). The depicted footprint scales not linearly with NIQ. This can be explained by a not linear size increase due to the specific requirements related with Tx technology (e.g. hybrid assembly at a single interface) and Tx performance (e.g. waveguide length adjustment sections for signal synchronization). For the sake of comparison, the area of an 8-ch Tx PIC is also shown in Figure 2.32 (red square). The ~30% footprint increase is caused by additionally integrated passive optical waveguide elements required for full Tx PIC fabrication (AWG, 1×8 splitter/combiner, length adjustment sections).

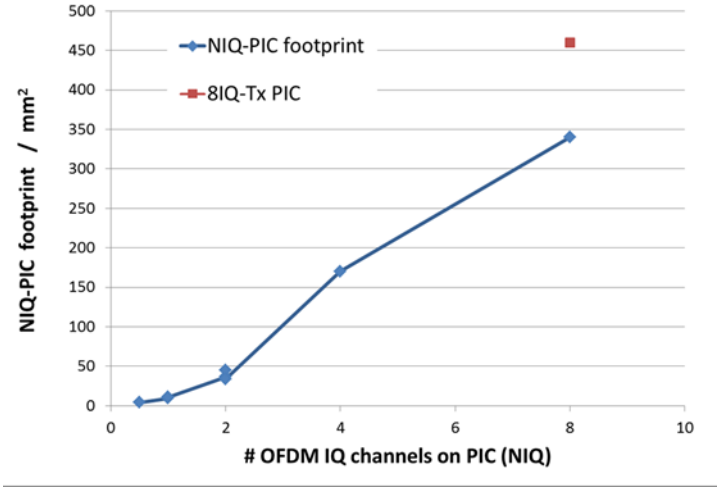


Figure 2.32 IQ PIC footprint as a function of the number of integrated IQ modulators NIQ (OFDM channels). The red square shows the size of a fully integrated 8-channel Tx PIC.

Based on the dependence of the N-channel IQ PIC footprint on the number of integrated IQ channels (NIQ) presented in Figure 2.32, the ideal number of available N-channel IQ PICs on a 3-inch wafer (Ni-PIC) was calculated (Figure 2.33, black graph). However, this plot does not account for the fact that rectangular-shaped devices need to be fitted on a circular wafer, which reduces additionally the overall available PIC volume with increasing PIC size (Figure 2.33, blue graph).

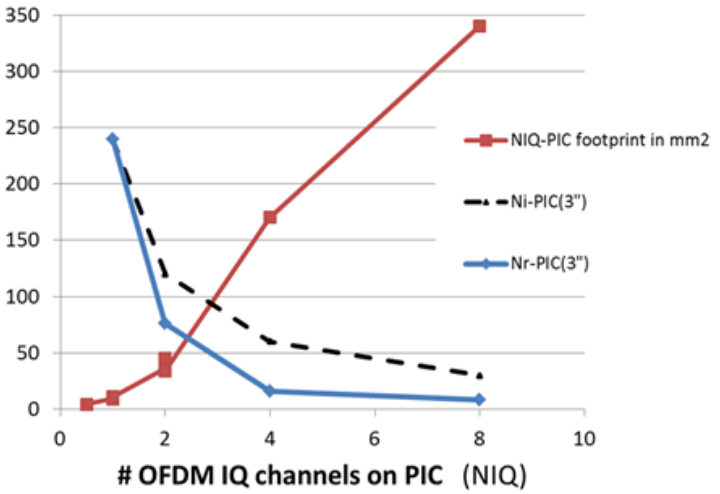


Figure 2.33 NIQ-PIC footprint (red), ideal number of NIQ-PICs (dashed black) and real number of NIQ-PICs (blue) on a 3-inch wafer vs. the number of integrated IQ modulators (OFDM channels).

So far on-wafer manufacturing yield related to given performance specifications was not considered, i.e. an ideal yield of 100% was assumed. Because no experimental data are available at present for such kind of very large-scale PIC fabrication, a simple and well-known mathematical relation was used to estimate possible yield data in a very first approximation:

$$Y_W(NIQ - PIC) = [Y_W(1IQ)]^{NIQ}$$

where:

Yw(NIQ-PIC): Yield of an N-channel IQ PIC (NIQ= 1,2,4,8)

NIQ: Number of IQ modulators (OFDM channels) integrated on PIC

Yw(1IQ): Yield of a single IQ modulator, NIQ=1 (1IQ = 2MZM), given by:

$$Y_W(1IQ) = [Y_W(1MZM)]^2$$

with:

Yw(1MZM): On-wafer yield of a single MZ modulator (1MZM) as parameter in Figure 2.34.

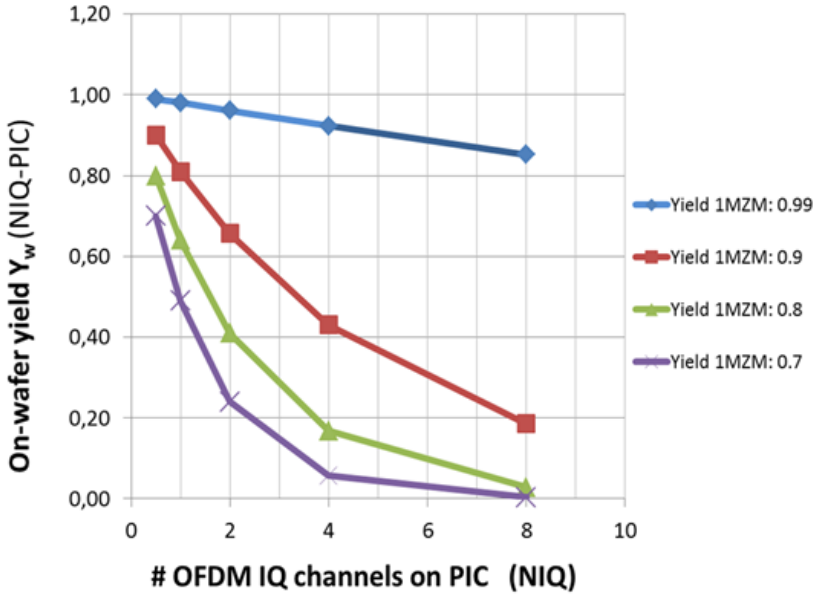


Figure 2.34 On-wafer NIQ-PIC yield vs. the number of integrated IQ modulators (NIQ) on PIC (Parameter: Single MZ modulator (1MZM) yield).

As can be seen from Figure 2.34, the final on-wafer PIC yield Y_W(NIQ-PIC) decreases with increasing number of integrated IQ modulators. Moreover, the negative slope depends very strongly on the achievable single MZ modulator yield. This simple estimation shows already that a maximum single MZM yield Y_W(1MZM) needs to be achieved (e.g. ≥ 90 %) in order to get acceptable production yields also for the large-scale 8-channel IQ PICs. In the case of the fully integrated Tx PIC, the overall NIQ-PIC yield is even lower because of additionally integrated passive optical waveguide elements (AWG, splitter/combiner) and the achievable fabrication yield of those.

Based on the estimations described above, the following question will be answered next: What is the cost increase at the wafer level caused by the fabrication of four 2ch-IQ PICs, two 4ch-IQ PICs or even one 8ch-IQ PIC in comparison with the fabrication of eight single IQ PICs (1ch-IQ) for final hybrid super-channel Tx assembly? The answer is given in Figure 2.35, which depicts the cost ratio of NIQ-PICs relative to eight single IQ MZ modulators (8× 1IQ) vs. the number of integrated IQ modulators (fabricated on a 3-inch InP wafer, for different single IQ (1IQ) on-wafer yields Y_W(1IQ)). As already seen in Figure 2.34, the fabrication yield Y_W(1MZM) of single MZ modulators –and thus the yield Y_W(1IQ) of single IQ PICs– has a very strong impact on the final overall NIQ-PIC yield, and therefore on cost. For example, if the 1IQ yield drops down to 80%, the fabrication cost of two 4ch-IQ PICs is ten times more than the cost for fabrication of eight single IQ PICs (Figure 2.35, 3-inch InP substrate). The cost ratio for one 8ch IQ PIC is ~20 more because the expected yield is already very low (Figure 2.34). As a consequence, the single IQ yield Y_W(1IQ) has to be > 80 % (!) in order to achieve still acceptable manufacturing cost also for integrated multiple IQ channels up to NIQ = 8. At this point it is noteworthy that, on the one hand, single IQs and 2ch-IQ PICs (Twin-IQ) enable higher fabrication yield and thus a better cost ratio than 4ch/8ch IQ PICs, but on the other, are not desirable for hybrid integration because of other avoidable issues (e.g. higher assembly/packaging effort and cost, larger Tx size, imperfect electrical RF connections)

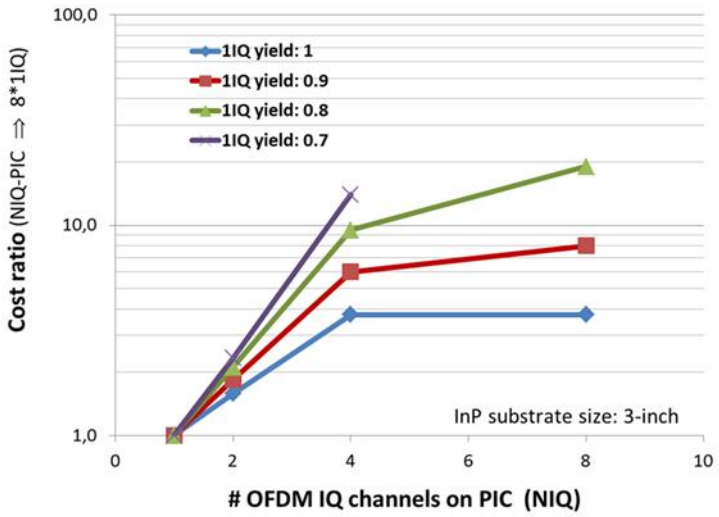


Figure 2.35 Cost ratio between the use of NIQ-PICs and the use of eight single IQs for hybrid 8-channel Tx fabrication (3-inch InP substrate, single IQ yield on-wafer as parameter).

In summary, solely monolithic integration of complex 4ch-and 8ch-IQ PICs –or even fully integrated 8ch-Tx PICs– on currently available 3-/4-inch InP substrates cannot reduce the fabrication cost of ASTRON's super-channel Tx even assuming that an ideal 100% fabrication yield could be feasible. On the contrary, the cost with respect to single MZ or IQ modulator production increases with increasing PIC footprint, and this increase is strongly dependent on the achievable manufacturing yields. Thus, from a cost perspective, a further strong improvement of InP manufacturing technologies in terms of repeatability, reliability and uniformity is the key requirement. The US company Infinera has already shown that monolithic large-scale InP Tx and Rx PIC fabrication is feasible for commercial telecom applications. The consequent improvement of InP technology and process control was the key to success. However, Infinera does not sell transceivers, as their cost would be prohibitive and not competitive. Instead, it sells transport systems which are effective in terms of cost and power as the monolithic integration of the optical equipment enhances OEO solutions for a simple system architecture fully adaptable to different network scenarios. Moreover, for larger PIC scales, like those currently developed and investigated in ASTRON, InP substrate sizes of $\geq$ 6-inch substrates are desirable to achieve economic very-large scale PIC production. But the commercial availability of InP substrates is limited to 3- and 4-inch at present. Thus, the application of monolithic integration technologies on larger Si substrates might be a promising alternative in future, provided that further progress is made on the development of Si-based photonic devices/PICs (e.g. IQ MZ modulators). Heterogeneous integration might be another promising option in future.

However, even with the estimated cost increase resulting from using currently available InP integration technology and substrate sizes for monolithic N-channel IQ PIC and Tx PIC fabrication, the monolithic/heterogeneous approach is an indispensable concept with a view to fabricating next generations of compact and very complex photonic components (e.g. Terabit OFDM Rx and Tx). This expectation is supported by the unquestionable potential advantages of these integration technologies:

- Large density of optical and electrical functions on smallest footprints
- Perfectly adapted and aligned optical and electrical interconnections between different functional devices
- Less optical and electrical interfaces to be connected by hybrid assembly (co-packaging), i.e. higher component yield and less overall cost at the backend fabrication level are expected.

These cost savings can also compensate for higher PIC cost at the wafer level (frontend level) to make compact components of high complexity available at a reasonable cost.

- Improved device reliability and robustness
- Improved device performance (e.g. RF bandwidth) and low power consumption
- Application of a single production line (technology).

Hybrid technologies (assembly, packaging) are still the key bottleneck towards economic photonic large scale/complexity component production. As a consequence, considerable cost reduction is expected for future commercial manufacturing due to

- Further improvement and increasing application of monolithic/heterogeneous integration technologies, thereby removing more and more photonic/electrical functions and interconnections from hybrid technology level (backend) onto chip level (frontend),
- Improvement of remaining indispensable hybrid process steps (cf. next subsection).

2.2.4.2 Co-packaging

In hybrid integration, the process steps whose yields have the biggest impact on cost are mainly the backend assembly steps, including weld, lidding and lid check, alignment and wire bond. In contrast, in monolithic integration the on-wafer technological processing steps (frontend processes), such as semiconductor layer growth, etching, deposition, and lithography, for example, have a greater impact [33].

Since backend processes (packaging and associated chip-to-board assembly) dominate the total cost of optical components, accounting for **at least 50% of total cost and up to 80%** for more complex devices, the consolidation of dozens of components into a single device creates significant efficiencies. Photonics packaging must provide optical input and output coupling as well as electronic connections and thermal management. Packaging reductions also save on costs associated with the individual burn-in and testing of many individual components. Optical coupling of the chip to a SMF is proving particularly troublesome. Existing automated high-throughput assembly tools have a placement accuracy of ±10μm, but single mode optics demand 1-2μm alignment tolerances [35]. Photonic integration therefore reduces the need for precise and complex sub-micron optical assemblies required to couple light from optical devices into optical fibre (and vice versa), and minimizes the time-consuming manual alignment and/or complex and costly robotic alignment systems required to do this, which can make final package costs be an order of magnitude more expensive than the chip itself. In addition, any change to a fibre attachment –due to manipulation, mechanical shock, vibration, or temperature shifts– reduces the performance of the component. Because of this, fibre couplings are the dominant potential failure point of today's optical components. Photonic integration can significantly reduce the number of fibre couplings in an optical transport system, thereby increasing system reliability and diminishing the impact of cumulative optical loss at each fibre-device interface, especially when many devices are cascaded. Furthermore, PIC-based systems' reliability can be further improved since their power levels can be decreased for the same system-level performance.

Even though integration can alleviate the problem of expensive manual fibre alignment and coupling, it does not solve it altogether and therefore new fibre-coupling techniques to connect photonic chips to SMF still need to be developed. Efforts have been made by the industry (Luxtera, Mellanox, Intel, or IBM) and research institutions (CEA-LETI (France), or Tyndall (Ireland)), which have come up with two strategies: grating couplers and edge couplers [35]. Grating couplers use diffraction to direct light upwards into a fibre above the chip surface. They encounter the problem of high spectral dependency (which limits their applicability to WDM systems) and low coupling efficiency. Currently, there exist commercial offerings by Luxtera. On the other hand, edge coupling uses an inverted taper to couple light between a horizontal fibre and the edge of the circuit. It offers a more efficient coupling and

broader spectral range, but matching the large optical mode of a SMF to the smaller mode of the Si waveguide is difficult and costly.

In either case, active alignment processes need to give way to fully automated or passive processes to reduce alignment time and cost. Beyond passive coupling, IBM has been developing fibre-coupling interfaces, such as polymer ribbons in which self-alignment ridges are lithographically defined in the coupling region of the polymer ribbon and silicon, such that when the ribbon and substrate are pressed together the placement improves from ±10μm to ±1-2μm. This has the advantage that fibre coupling can be realised using standard high-volume, low-cost microelectronic packaging equipment [35].

Finally, functional on-chip testing can be performed at a wafer level if diagnostic devices are integrated in a PIC. This allows performing in-situ testing and screening before incurring costs for device separation, mounting and testing.

Taking all this into consideration, and using the results of subsection 2.2.4.1, the integration (including packaging) reduction factor of 0.4 assumed in the transceiver cost model presented in sections 2.1.2, 2.2.1 and 2.2.2 would be possible if the packaging and assembly accounts for ~55% of the transceiver cost and the 1IQ yield is 1. For lower yields, according to the results shown in Figure 2.35, the integration reduction factor should be decreased and the percentage of transceiver cost due to packaging and assembly should be approximated to a value closer to the 80% of the total transceiver cost indicated above on account of the complexity of the ASTRON transceiver solutions. In fact, if packaging represents 70% of the total super-channel cost, an integration reduction factor of 0.4 would still be possible if 1IQ yield equals 0.9, and, likewise, if the packaging is 77% of the total super-channel cost, the 1IQ yield could decrease to 0.8. These percentages can be reduced to 65% and 72%, for yields equal to 0.9 and 0.8, respectively, if the integration cost reduction factor is scaled down to 0.1. In the sensitivity analysis carried out in the next section, we will vary the integration reduction factor to take into account different costs of the backend processes in our cost reference model.

2.3 Sensitivity analysis and comparison of transceiver implementation solutions in terms of cost and power consumption

Several factors can affect the transceiver cost. On the one hand, the DSP cost represents 45-50% of super-channel transceiver cost (with 4-12 sub-channels). However, the DSP cost can be reduced by up to 75-85% by shrinking the die size, as we saw above, if the nodes go from current 40nm to 16 nm CMOS technology. Furthermore, higher costs will result for companies without in-house DSP manufacturing capability. On the other hand, packaging savings and the advent of new electro-optical integration platforms, e.g. silicon photonics, may also have a strong impact on the transceiver cost.

This variation of cost needs to be taken into account in the cost and power consumption model presented in this document. To summarise and compare the different transceiver implementations described in this chapter, in Figure 2.36(a) we present a sensitivity analysis of the cost of the super-channel transceiver (assuming eight sub-channels per super-channel) on the HSR filter cost. We observe that the transceivers with all-optical filtering can be the most cost-effective. The NWDM transceiver based on the N×1 HSR filter exhibits the lowest cost in the entire HSR filter cost range and decreases steadily with the HSR filter cost, but not as rapidly as the transceiver based on the 1×1 HSR filter, which is always more expensive than the N×1 HSR filter transceiver implementation because four 1×1 HSR filters are needed. When the 1×1 HSR filter costs 1.15 times the cost of a 1×9 WSS, the NWDM transceiver based on the 1×1 HSR filter becomes more cost-effective than any of the transceiver implementations based on digital filtering (i.e. NFDM –which is a NWDM transceiver with digital filtering–, eOFDM and conventional AOFDM). The ASTRON solutions, i.e. OS-OFDM and AO-OFDM with DSP in the receiver, would have the same performance as NFDM/eOFDM and AO-OFDM, respectively).

This study was carried out assuming an integration cost reduction factor (ICRF) equal to 0.4. In Figure 2.36(b) we present the results of a sensitivity analysis on the ICRF. We observe that AO-OFDM and

NFDM/eOFDM/OS-OFDM become more cost-effective than NWDM with N×1 HSR (with current cost = 0.72) when ICRF > 0.5 and achieve the same cost as NWDM with 1×1 HSR (with potential future cost = 0.22) if ICRF = 0.7. On the contrary, if ICRF < 0.2, the transceiver implementations based on optical filtering are always more cost-effective even at current costs of ultra-fine-granularity HSR filters, where a cost premium due to new technology development has been considered. This points up the importance of integration and packaging in making the ASTRON-project super-channel transceivers viable.

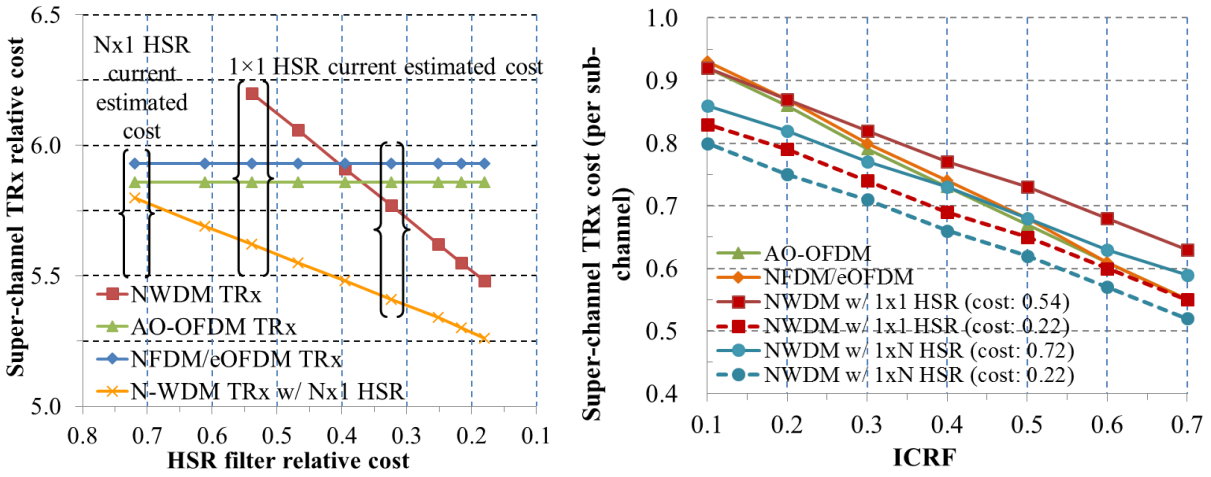


Figure 2.36 Sensitivity analysis of the relative cost of a super-channel transceiver composed of 8 sub-channels for electrical multiplexing schemes (NFDM/eOFDM), NWDM with optical filtering (with either two 1×1 HSR filters and an interleaver, as shown in Figure 2.3, or with one Nx1 HSR filter) and conventional AO-OFDM (according to the design presented in Figure 2.4) on (a) the relative cost of the HSR filter and (b) the integration cost reduction factor (ICRF) accounting for chip integration and packaging savings. The HSR filter cost is assumed to vary from a relative cost of 0.54 (current estimated cost of a 1×20 WSS) to ~0.2. For reference, we also indicated the current cost of a 1x9 WSS. The ICRF has been varied from 0.1 to 0.7 of the cost of the components mentioned in subsection 2.1.2.1. Shown are relative costs to 100G transceiver cost.

In Figure 2.37 we present the relative cost per sub-channel of a super-channel (Sp-Ch) transceiver as a function of the DSP cost. We used the relative cost of the DSP in a single-carrier transceiver (0.36) as a reference and varied the DSP cost from 0.1 to 0.6. We observed that by increasing the DSP cost from 0.36 to 0.5 the cost of the super-channel transceiver would increase by 38% (if ICRF = 0.4) or 31% (if ICRF = 0.1). Similarly, if the DSP cost is decreased from 0.36 to 0.2, the cost of the super-channel transceiver would decrease by 27% (if ICRF = 0.4) or 22% (if ICRF = 0.1). As for the fraction of the super-channel transceiver cost that is attributed to the DSP, it increases from 39% (if ICRF = 0.1) or 49% (if ICRF = 0.4) for the reference DSP cost value of 0.36 to 53% (if ICRF = 0.1) or 63% (if ICRF = 0.4) for a DSP cost of 0.5. If, on the other hand, the DSP cost could be lowered to 0.2, the DSP cost would represent 22% (if ICRF = 0.1) or 30% (if ICRF = 0.4).

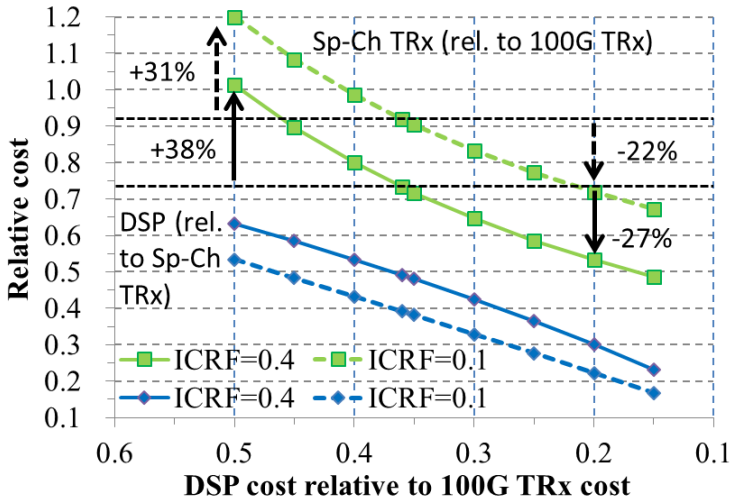


Figure 2.37 Relative cost per sub-channel of a super-channel transceiver composed of 8 sub-channels according to the AO-OFDM design presented in Figure 2.4 (green curves) and fraction of total transceiver cost due to DSP (blue curves) as a function of the relative cost of the DSP. The super-channel and DSP costs are relative to the cost of a 100G transceiver. Two ICRF values (0.4 and 0.1) have been considered. We have taken 0.36 as a reference for the DSP cost, according to Table 2.1.

In Table 2.20 we present the relative cost per sub-channel of super-channel transceiver implementations supporting different numbers of sub-channels. We can observe that, by using super-channel transceivers, a substantial reduction in the relative cost of transmitting one sub-channel, with respect to the cost of transmitting single-carrier signals (100G transceiver cost = 1), can be achieved. From a cost perspective, it is clear that in a heterogeneous traffic scenario in which a majority of the connections is not sufficiently big to justify the exclusive use of a super-channel to serve a single connection, we can anticipate that using super-channel transceivers at the source and destination nodes to serve connections from the source node to the end node and any intermediate nodes, as well as from any intermediate node to the end node, together with the capability of extracting and adding sub-channel constituents from/to super-channels at the intermediate nodes should be beneficial. This will be assessed in chapter 3 with the aid of the new ROADM architectures with all-optical sub-channel add/drop capability described in section 2.4.

Table 2.20 Super-channel transceiver relative cost and power (per sub-channel) for implementations supporting from 4 to 12 sub-channels. Relative costs to cost of 100G transceiver.

	NFDM/eOFDM		NWDM		AO-OFDM	
Number of sub-channels	Cost	P (W)	Cost	P (W)	Cost	P (W)
4	0.80	50.8	0.98	52.8	0.79	50.8
6	0.76	49.2	0.84	50.5	0.75	49.2
8	0.74	48.4	0.77	49.4	0.73	48.4
10	0.73	47.9	0.73	48.7	0.72	47.9
12	0.72	47.6	0.71	48.3	0.71	47.6

To conclude this section, we evaluate the impact of the DSP power consumption on the overall super-channel transceiver power consumption. Figure 2.38 shows the power reduction in a super-channel

transceiver with eight sub-channels due to reductions in DSP power consumption with respect to the reference value of 308W for an MB-eOFDM transceiver provided in Table 2.6. We have shown that a reduction of ~20% due to DSP sub-banding, as shown in Table 2.12 for ASTRON's OS-OFDM super-channel transceiver can bring an overall transceiver power reduction of ~18%. Further power reduction can be achieved through advances in soft-decision FEC and semiconductor technologies.

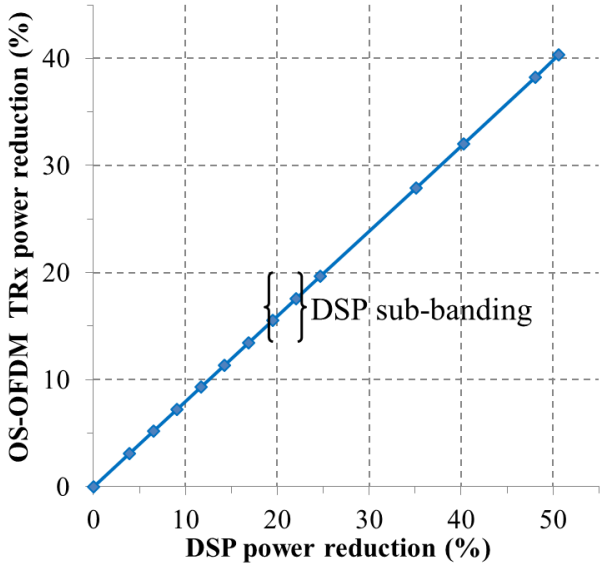


Figure 2.38 Power reduction attainable in an OS-OFDM super-channel transceiver due to reductions in DSP power consumption. We have highlighted the value given in Table 2.12 due to DSP sub-banding. Further power reduction can be achieved through advances in soft-decision FEC.

2.4 Flexible ROADM designs

Two ROADM implementations have been considered in the cost and power consumption reference model: a colourless, contentionless ROADM and a colourless, directionless ROADM. Both implementations are based on a route and select (R&S) architecture with built-in flex-grid WSSs. The case of colourless, directionless, contentionless ROADMs, though arousing increasing interest from telecom operators, is regarded as a distant-future solution and has not been taken into account, especially because it is not clear what will be the preferred technology for the A/D stage (multi-cast switches or M×N WSSs).

2.4.1 Colourless, contentionless ROADM

2.4.1.1 Conventional ROADM

A conventional colourless, contentionless R&S ROADM architecture without all-optical sub-channel add/drop capability is shown in Figure 2.39. It incorporates commercially available flexible 1×20 WSS with relatively coarse 7.5-GHz optical resolution, 6.25-GHz pixel spectral addressability and insertion loss (IL) < 5 dB, for super-channel routing.

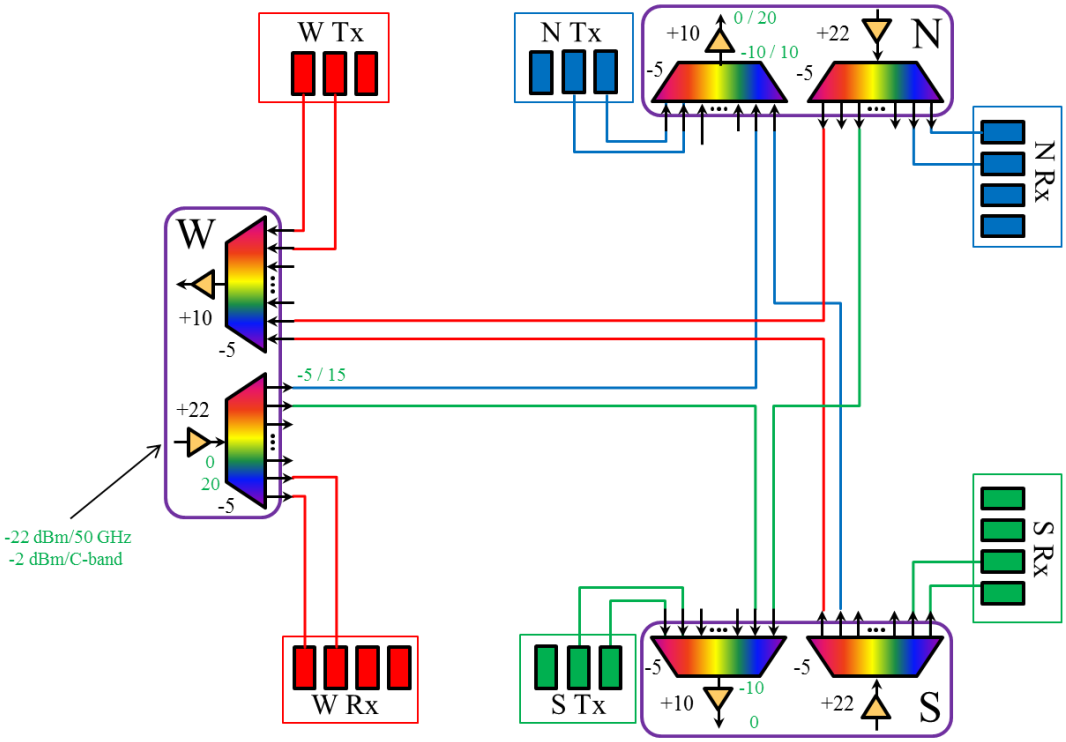


Figure 2.39 Design of a conventional colourless, contentionless R&S ROADM with degree *D* = 3. Shown is the total optical power (over 50GHz bandwidth and the entire C-band) at different locations together with insertion loss values of the different node components.

The conventional ROADM cost with respect to the cost of a 100G transceiver (*C*) and power consumption (*P*) values are given by the following expressions as a function of the nodal degree *D*:

$$C = (2C_{WSS} + 0.18)D, \quad (1)$$

$$P(W) = 20D - 12PRF(D-1), \quad (2)$$

where PRF is the power reduction factor, shown in Table 2.21 with a value of 0.1. This factor accounts for the fact that some of the control and management can be shared between the different amplification modules present within a node. In the power model we have assumed that this 10% power reduction can be applied to all amplifiers minus 1. We can achieve more power reduction by sharing the same pump laser between different EDFAs. A common pump is simply divided *D*-ways and a cheap VOA is added to each copy to control power/gain. The pump sharing scenario is expected to give an additional 30% power reduction per node. This translates into an overall node power consumption of 50.4W for a 3-degree node, which represents a reduction of 12.5% with respect to the estimation shown in Table 2.21.

Table 2.21 Cost and power consumption of a conventional colourless, contentionless R&S ROADM with degree D =3. (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver. (^) Due to sharing of management between amplification modules.

Component	Relative Unit cost (*)	Power (W)	#	Relative cost (*)	Relative cost (**)	Power reduction factor (^)	Total Power (W)
WSS	0.54	4.00	6	3.2	16.9		24.0
Variable gain dual-stage amplifier	0.18	12.0	3	0.5	2.8	0.10	33.6
				3.8	19.7		57.6

2.4.1.2 ROADM with all-optical sub-channel add/drop capability

The R&S ROADM architecture with all-optical sub-channel add/drop capability is shown in Figure 2.40 and Figure 2.41. It is based on a commercially available flexible 1×20 WSS with relatively coarse 7.5-GHz optical resolution, 6.25-GHz pixel spectral addressability and insertion loss (IL) < 5 dB, for super-channel routing. The A/D cards are realised with either an HSR filter with 0.8-GHz resolution, 400-MHz addressability and IL ~15 dB [13], or a Terabit interferometric drop, add and extract (TIDE) processor [36], fully flexible in selecting any centre frequency throughout the C-band. With NWDM/MB-eOFDM, A/D cards use one HSR filter. With AO-OFDM, due to the overlapping Sb-Chs, we require A/D cards with two HSR shaping filters (for single-gated TIDE processor) or two 1×*G* HSR filters (for a solution comprising *G* gates), along with an additional amplifier.

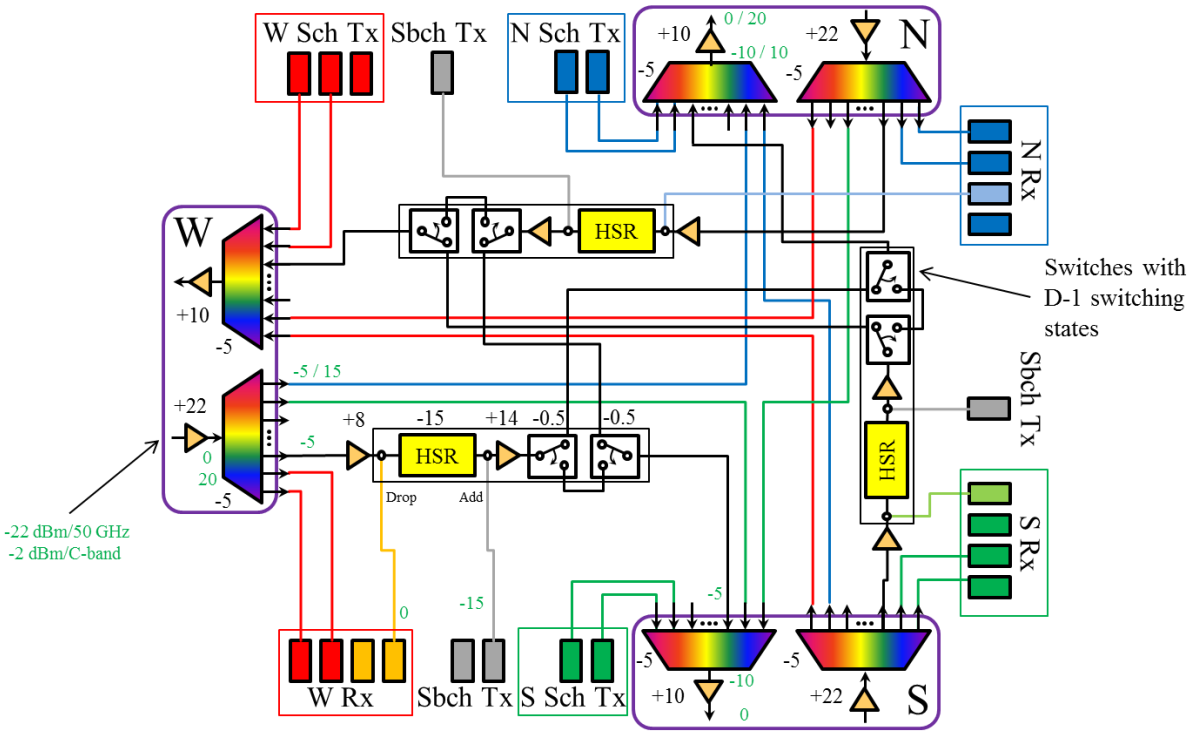


Figure 2.40 Design of a colourless, contentionless R&S ROADM with degree *D* = 3 incorporating three all-optical sub-channel add/drop cards for non-overlapping sub-channels. Shown is the total optical power (over 50GHz bandwidth and the entire C-band) at different locations together with insertion loss values of the different node components.

Based on the relative cost (with respect to the cost of a 100G transceiver) and power consumption of the ROADM components, we can estimate the overall cost (*C*) and power consumption (*P*) of the ROADM with all-optical sub-channel add/drop capability for non-overlapping sub-channels

$$C = (2C_{WSS} + 0.18)D + [C_{HSR} + 0.18 + 0.02(1 - \delta_{D2})]M, \quad (3)$$

$$P(W) = 20D + 16M - 12PRF(D + M - 1), \quad (4)$$

and the ROADM with all-optical sub-channel add/drop capability for overlapping sub-channels

$$C = (2C_{WSS} + 0.18)D + [2C_{HSR} + GC_{GATE} + 0.29 + 0.02(1 - \delta_{D2})]M, \quad (5)$$

$$P(W) = 20D + (29 + 4G)M - 12PRF[D + (21/12)M - 1], \quad (6)$$

where C_{WSS}, C_{HSR}, and C_{GATE} represent the relative cost of a 1×20 WSS, a 1×1 HSR filter (or a 1×*G* HSR filter if *G*>1, where *G* is the number of gates per card), and a TIDE gate, indicated in Table 2.22 and Table 2.23; δ_{D2} is the Kronecker delta, equal to 1 when *D* = 2; and *PRF* is a power reduction factor accounting for the fact that some of the control and management can be shared between the different amplification modules within the node.

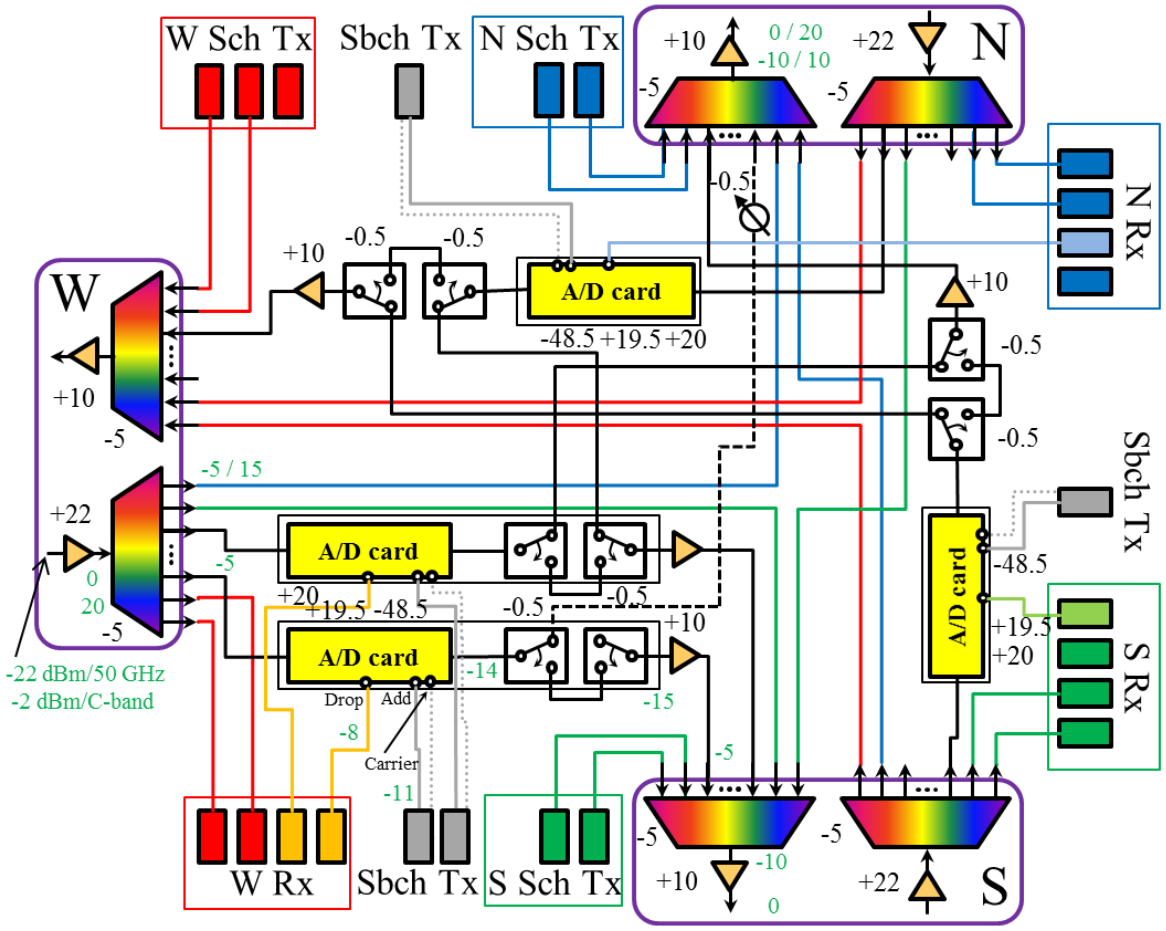


Figure 2.41 Design of a colourless, contentionless R&S ROADM with degree *D* = 3 incorporating four all-optical sub-channel add/drop cards for overlapping sub-channels. Shown is the total optical power (over 50GHz bandwidth and the entire C-band) at different locations together with insertion loss values of the different node components.

In Table 2.22 and Table 2.23 we present the cost and power consumption of each ROADM component and calculate the total relative cost and power consumption for a ROADM with degree *D* = 3 and three sub-channel A/D cards for the cases in which sub-channels are non-overlapping and overlapping. We observe that the ROADM for the first case is significantly more cost-effective, especially if the number of sub-channel A/D cards increases. This is due to the fact that for overlapping signals we need twice as many HSR filters as in the case of non-overlapping signals, to perform the FFT and iFFT in order to do the selection of the sub-channel that will later be dropped [36].

Table 2.22 Cost and power consumption of a conventional colourless, contentionless R&S ROADM with degree *D* =3 and number of non-overlapping sub-channel add/drop cards M = 3. (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver. (***) Cost relative to cost of a conventional ROADM with degree D = 3. (^) Due to sharing of management between amplification modules.

Component	Relative unit cost (*)	Power (W)	#	Relative cost (*)	Relative cost (**)	Relative cost (***)	Power reduction factor (^)	Total Power (W)

WSS	0.54	4.00	6	3.24	16.92	0.86		24.0
1x1 HSR filter	0.54	4.00	3	1.62	8.46	0.43		12.0
Variable gain dual-stage amplifier	0.18	12.00	6	1.08	5.64	0.29	0.10	66.0
1x(D-1) switch	0.01	0.00	6	0.09	0.45	0.02		0.0
				6.02	31.47	1.59		102.0

Table 2.23 Cost and power consumption of a conventional colourless, contentionless R&S ROADM with degree *D* =3 and number of overlapping sub-channel add/drop cards M = 3. (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver. (***) Cost relative to cost of a conventional ROADM with degree D = 3. (^) Due to sharing of management between amplification modules.

Component	Relative unit cost (*)	Power (W)	#	Relative cost (*)	Relative cost (**)	Relative cost (***)	Power reduction factor (^)	Total Power (W)
WSS	0.54	4.00	6	3.24	16.92	0.86		24.0
1x1 HSR filter	0.54	4.00	6	3.24	16.92	0.86		24.0
Integrated TIDE gate	0.11	4.00	3	0.32	1.69	0.09		12.0
Variable gain amplifier	0.11	9.00	3	0.32	1.69	0.09	0.10	24.3
Variable gain dual-stage amplifier	0.18	12.00	6	1.08	5.64	0.29	0.10	66.0
1x(D-1) switch	0.01	0.00	6	0.09	0.45	0.02		0.0
				8.29	43.31	2.19		150.3

2.4.2 Colourless, directionless ROADM

2.4.2.1 Conventional ROADM

A conventional colourless, directionless R&S ROADM architecture without all-optical sub-channel add/drop capability is shown in Figure 2.42. It incorporates commercially available flexible 1×20 WSS with relatively coarse 7.5-GHz optical resolution, 6.25-GHz pixel spectral addressability and insertion loss (IL) < 5 dB, for super-channel routing. Unlike the colourless, contentionless design depicted in Figure 2.39, the A/D stage is common for all ROADM degrees and it is composed of four 1×20 WSS, two for the Add part and two for the Drop part, as observed at the bottom of Figure 2.42.

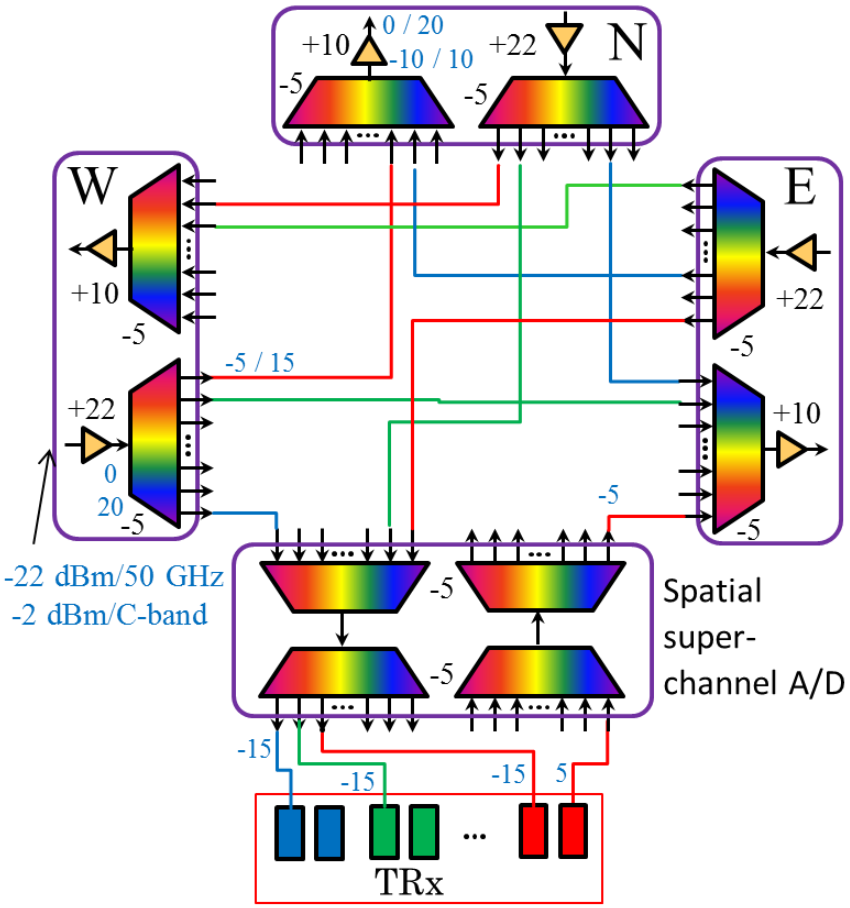


Figure 2.42 Design of a conventional colourless, directionless R&S ROADM with degree *D* = 3. Shown is the total optical power (over 50GHz bandwidth and the entire C-band) at different locations together with insertion loss values of the different node components.

The conventional ROADM cost with respect to the cost of a 100G transceiver (*C*) and power consumption (*P*) values are given by the following expressions as a function of the nodal degree *D*:

$$C = \left[\left(2 + \frac{4}{D}\right) C_{WSS} + 0.18\right] D, \quad (7)$$

$$P(W) = 20D - 12PRF(D-1) + 16, \quad (8)$$

where PRF is the power reduction factor, shown in Table 2.24 with a value of 0.1. In Table 2.24

Table 2.24 Cost and power consumption of a conventional colourless, directionless R&S ROADM with degree *D* =3. (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver. (***) Cost relative to cost of a conventional ROADM with degree D = 3. (^) Due to sharing of management between amplification modules.

Component	Relative Unit cost (*)	Power (W)	#	Relative cost (*)	Relative cost (**)	Power reduction factor (^)	Total Power (W)
WSS	0.54	4.00	10	5.4	28.2		40.0
Variable gain dual-stage amplifier	0.18	12.0	3	0.5	2.8	0.10	33.6
				5.9	31.0		73.6

2.4.2.2 ROADM with all-optical sub-channel add/drop capability

The R&S ROADM architecture with all-optical sub-channel add/drop capability is shown in Figure 2.43 and Figure 2.44.

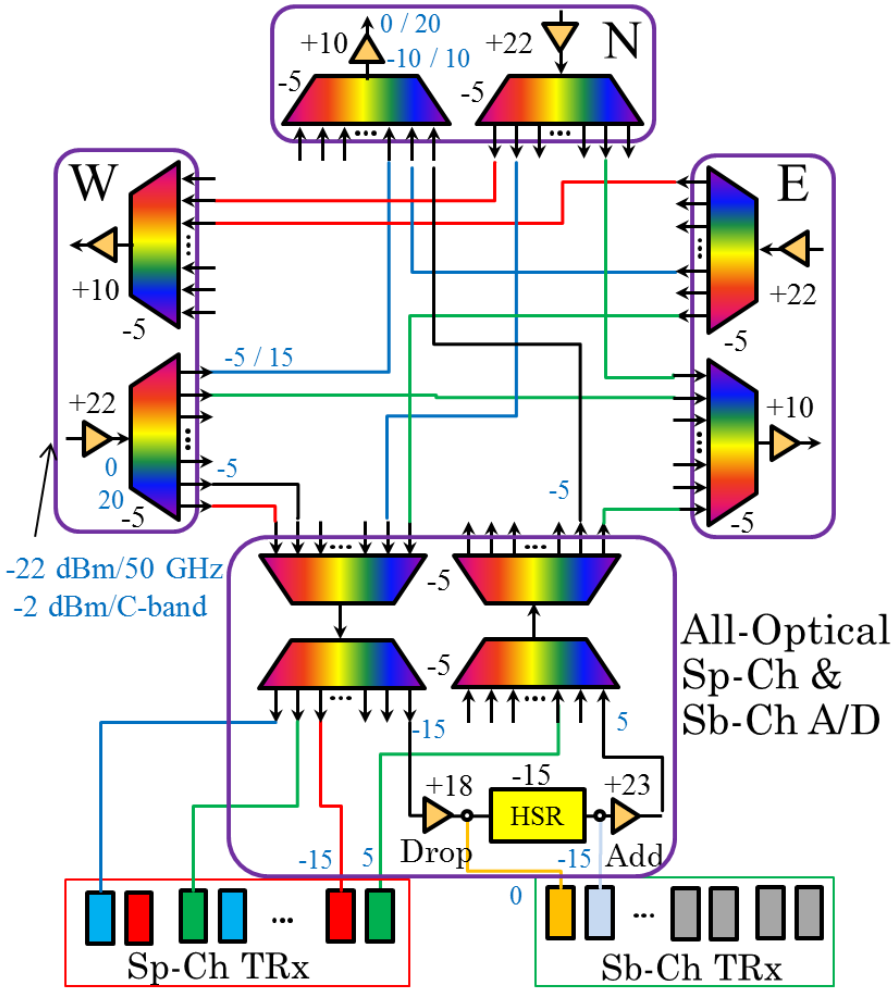


Figure 2.43 Design of a colourless, directionless R&S ROADM with degree *D* = 3 with all-optical sub-channel add/drop capability for non-overlapping sub-channels. Shown is the total optical power (over 50GHz bandwidth and the entire C-band) at different locations together with insertion loss values of the different node components.

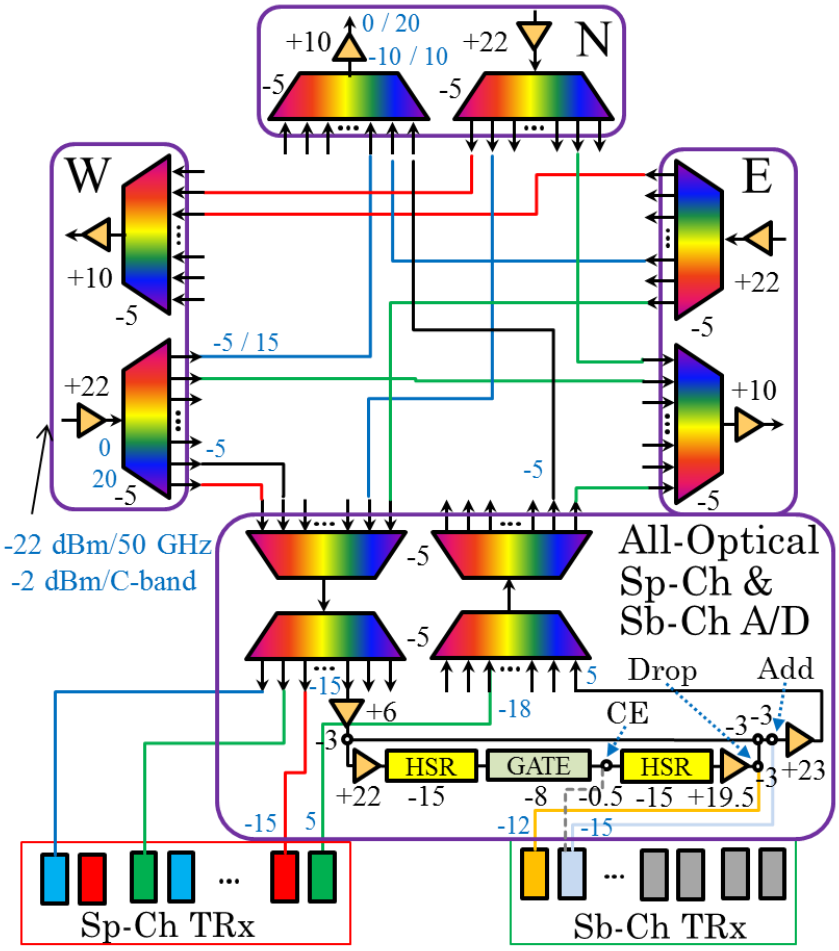


Figure 2.44 Design of a colourless, directionless R&S ROADM with degree *D* = 3 with all-optical sub-channel add/drop capability for overlapping sub-channels. Shown is the total optical power (over 50GHz bandwidth and the entire C-band) at different locations together with insertion loss values of the different node components.

Based on the relative cost (with respect to the cost of a 100G transceiver) and power consumption of the ROADM components, we can estimate the overall cost (*C*) and power consumption (*P*) of the ROADM with all-optical sub-channel add/drop capability for non-overlapping sub-channels

$$C = \left[\left(2 + \frac{4}{D}\right) C_{WSS} + 0.18\right] D + (C_{HSR} + 0.18)M, \quad (9)$$

$$P(W) = 20D + 16(M + 1) - 12PRF(D + M - 1), \quad (10)$$

and the ROADM with all-optical sub-channel add/drop capability for overlapping sub-channels

$$C = \left[\left(2 + \frac{4}{D}\right) C_{WSS} + 0.18\right] D + (2C_{HSR} + GC_{GATE} + 0.36)M, \quad (11)$$

$$P(W) = 20D + (32 + 4G)M - 12PRF[D + 2M - 1] + 16\,, \quad (12)$$

where C_{WSS}, C_{HSR}, and C_{GATE} represent the relative cost of a 1×20 WSS, a 1×1 HSR filter (or a 1×*G* HSR filter if *G*>1, where *G* is the number of gates per card), and a TIDE gate, indicated in Table 2.25 and Table 2.26; and *PRF* is a power reduction factor accounting for the fact that some of the control and management can be shared between the different amplification modules within the node.

In Table 2.25 and Table 2.26 we present the cost and power consumption of each ROADM component and calculate the total relative cost and power consumption for a ROADM with degree *D* = 3 and three sub-channel A/D cards for the cases in which sub-channels are non-overlapping and overlapping.

Table 2.25 Cost and power consumption of a conventional colourless, directionless R&S ROADM with degree *D* =3. (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver. (***) Cost relative to cost of a conventional ROADM with degree D = 3. (^) Due to sharing of management between amplification modules.

Component	Relative unit cost (*)	Power (W)	#	Relative cost (*)	Relative cost (**)	Relative cost (***)	Power reduction factor (^)	Total Power (W)
WSS	0.54	4.00	10	5.40	28.20	1.43		40.0
1x1 HSR filter	0.54	4.00	3	1.62	8.46	0.43		12.0
Variable gain dual-stage amplifier	0.18	12.00	6	1.08	5.64	0.29	0.10	66.0
				8.09	42.29	2.14		118.0

Table 2.26 Cost and power consumption of a conventional colourless, directionless R&S ROADM with degree *D* =3. (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver. (***) Cost relative to cost of a conventional ROADM with degree D = 3. (^) Due to sharing of management between amplification modules.

Component	Relative unit cost (*)	Power (W)	#	Relative cost (*)	Relative cost (**)	Relative cost (***)	Power reduction factor (^)	Total Power (W)
WSS	0.54	4.00	10	5.40	28.20	1.43		40.0
1x1 HSR filter	0.54	4.00	6	3.24	16.92	0.86		24.0
Integrated TIDE gate	0.11	4.00	3	0.32	1.69	0.09		12.0
Variable gain dual-stage amplifier	0.18	12.00	9	1.62	8.46	0.43	0.10	98.4
				10.58	55.26	2.80		174.4

2.4.3 Sensitivity analysis and comparison of ROADM architectures

In Figure 2.45 we compare the cost of the different colourless, contentionless ROADM architectures with all-optical sub-channel A/D capability assuming a nodal degree D = 2.9 and a number of sub-channel A/D cards M = 1 (average values in the France Telecom network used in chapter 3). For reference, we have also included in the graph the cost of the super-channel transceivers, as shown in Figure 2.36(a). We observe that the cost of the ROADM decreases steeply as the cost of the 1×1 HSR filter/1×20 WSS decreases.

In Figure 2.46 we present the same results for the colourless, directionless ROADM architectures, including the conventional ROADM without all-optical sub-channel A/D capability. In this case, the ROADMs have a higher cost than the transceivers with current 1×1 HSR filter/1×20 WSS costs, but this can be reduced to 0.4-0.5 times the cost of a transceiver if the cost of a 1×1 HSR filter/1×20 WSS could be brought down to that of a 1×9 WSS.

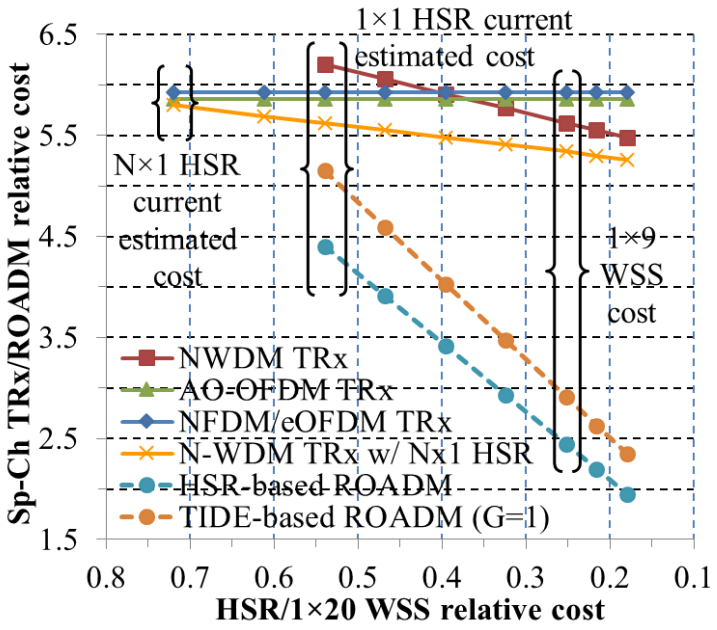


Figure 2.45 Sensitivity analysis of the relative cost of a super-channel transceiver composed of 8 sub-channels for electrical multiplexing schemes (NFDM/eOFDM), NWDM with optical filtering (with either two 1×1 HSR filters and an interleaver, as shown in Figure 2.3, or with one Nx1 HSR filter) and conventional AO-OFDM (according to the design presented in Figure 2.4), as well as a colourless, contentionless R&S ROADM with all-optical sub-channel A/D capability for non-overlapping (HSR-based) and overlapping (TIDE-based) sub-channels on the relative cost of the HSR filter/1×20 WSS. The HSR filter/1×20 WSS relative cost is assumed to vary from 0.54 (current estimated cost of a 1×20 WSS) to ~0.2. For reference, we also indicated the current cost of a 1x9 WSS. This graph was plotted assuming a nodal degree D = 2.9 and a number of sub-channel A/D cards M = 1 (average values in the France Telecom network used in chapter 3). For the transceivers, we assumed ICRF = 0.4 and a DSP cost of 0.36. Shown are relative costs to 100G transceiver cost.

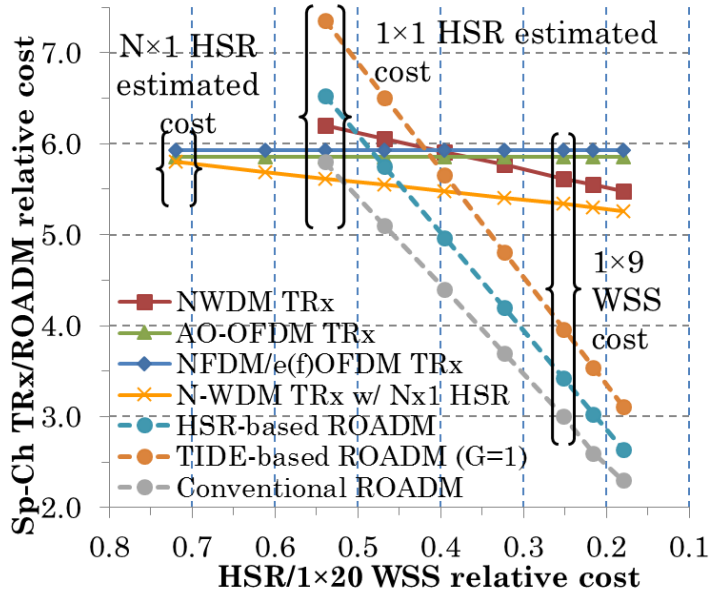


Figure 2.46 Sensitivity analysis of the relative cost of a super-channel transceiver composed of 8 sub-channels for electrical multiplexing schemes (NFDM/eOFDM), NWDM with optical filtering (with either two 1×1 HSR filters and an interleaver, as shown in Figure 2.3, or with one N×1 HSR filter) and conventional AO-OFDM (according to the design presented in Figure 2.4), as well as a colourless, directionless R&S ROADM, either conventional or with all-optical sub-channel A/D capability for non-overlapping (HSR-based) and overlapping (TIDE-based) sub-channels, on the relative cost of the HSR filter/1×20 WSS. The HSR filter/1×20 WSS relative cost is assumed to vary from 0.54 (current estimated cost of a 1×20 WSS) to ~0.2. For reference, we also indicated the current cost of a 1x9 WSS. This graph was plotted assuming a nodal degree D = 2.9 and a number of sub-channel A/D cards M = 1 (average values in the France Telecom network used in chapter 3). For the transceivers, we assumed ICRF = 0.4 and a DSP cost of 0.36. Shown are relative costs to 100G transceiver cost.

In Figure 2.47 we carry out a sensitivity analysis of the influence of the number of sub-channel (Sb-Ch) A/D cards per ROADM on the colourless, directionless ROADM cost. We observe that with just one sub-channel A/D card the cost of the ROADM only increases by <20%, but it could become more than twice the cost of a conventional ROADM as the number of sub-channel A/D cards *M* increases. This is usually the case in ROADMs with low number of degrees *D*, whereas the impact of the number of sub-channel A/D cards is reduced as *D* increases. For *D* = 5, the cost increase can be as little as 8.5% with *M* = 1 and grows to 51% with *M* = 6, if we assume a 1×1 HSR filter/1×20 WSS cost = 0.22.

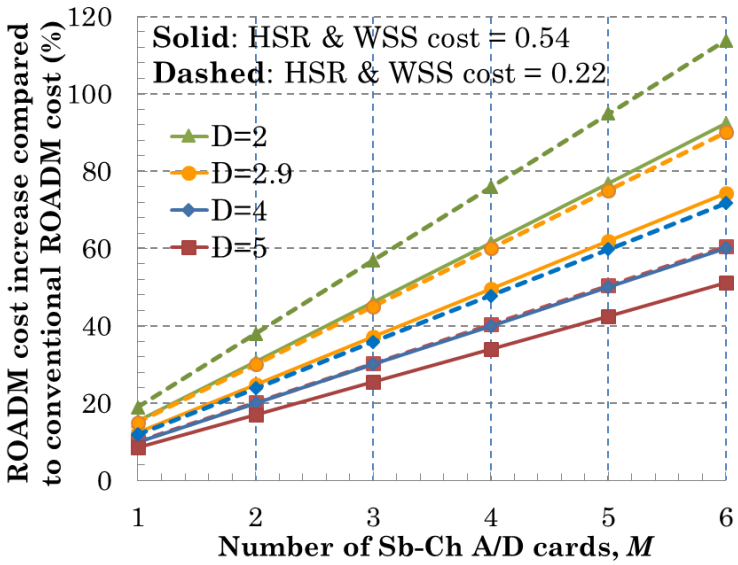


Figure 2.47 Sensitivity analysis of the cost increase of a colourless, directionless R&S HSR-based ROADM with all-optical sub-channel A/D capability with respect to a convention colourless, directionless R&S ROADM on the number of sub-channel A/D cards *M*. The study has been done for different nodal degrees and HSR filter/1×20 WSS costs.

3. Network-level performance evaluation

3.1 Introduction

Despite the potential performance enhancements that the introduction of a new technology may have, operators seeking to migrate to next-generation optical networks are likely to select a solution by taking the required capital expenditures into account. This chapter aims to evaluate the expected improvement of performance and cost saving introduced by the ASTRON technology from the networking perspective. All studies are carried out over the network topology described in section 3.2. Legacy technologies, as detailed in section 3.3, are used for benchmarking purposes. The scenarios based on the ASTRON solutions, along with a traffic grooming capable routing and spectrum allocation algorithm [37] are introduced in section 3.4. Finally, section 3.5 presents the techno-economic study methodology and results.

3.2 Reference network topologies and characteristics

This section describes the reference network as well as the traffic demands used for the feasibility, techno-economic and energy consumption analysis. The reference network is a national-scale backbone network (France Telecom national network).

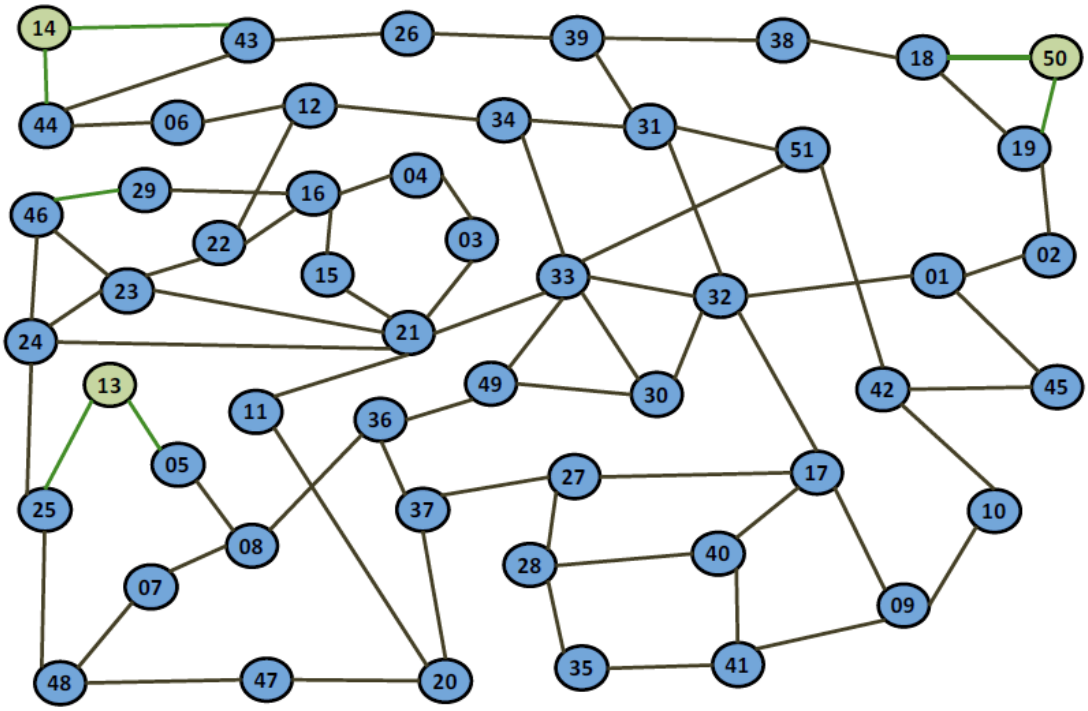


Figure 3.1 The France Telecom national network.

Figure 3.1 depicts the France Telecom national network topology, which is representative of a typical transmission backbone network encountered in a European country. The network is composed of 51 nodes connected together through 75 links, each of them having a pair of fibres (one fibre per direction). Although the mean nodal degree in this topology is 2.9, note that 3 out of the 51 nodes (nodes 21, 32 and 33) have a rather high degree of meshing, which makes this topology an interesting case for study. The majority of links (80%) are shorter than 300 km, with 25% of links shorter than 50 km, usually corresponding to intra-city links. However, two links in this topology (among the links represented in green in Figure 3.1) are much longer than the average (1,300 km and 2,427 km). Furthermore, it is worth mentioning that the whole C-band (4.8 THz) has been considered on all network links. For more details please go to [38].

3.3 Benchmarking cases

In the following, we describe the benchmarking scenarios under study. Two options are considered: a single-line-rate (SLR) transmission system over 50-GHz grid (which represents the current state of deployed optical networking technology) and a multi-line-rate (MLR) transmission system over flexi-grid.

The SLR scenario, as shown in Figure 3.2, employs a single type of transceiver to serve all demands over the network and therefore the selected modulation format should be able to guarantee the quality of transmission (QoT) of all connection requests at the receiver side. In this study, we have chosen DP-BPSK for the SLR case, since it is the most commonly deployed modulation format in coherent 100G transmission systems. Moreover, we assume transmission on the fixed 50-GHz ITU-T frequency grid.

To solve the routing sub-problem, the fixed-alternate-routing (FAR) approach was adopted, which considers K-disjoint (K = 3) routes between source-destination pairs. Each node in the network maintains a routing table that contains an ordered list of routes to each destination node. The routes include the shortest, the second-shortest and the third-shortest path calculated by Dijkstra's algorithm from the source node *s* to the destination node *d*. It is important to note that a link-disjoint approach has been applied in the path calculations, i.e. the second-shortest path between *s* and *d* is any route that does not share any links (is *link-disjoint*) with the shortest path. In the same way, the third-shortest path is any link-disjoint route with already existing routes (shortest and second-shortest path) in the routing table of *s*. Note that the maximum number of possible routes between each source-destination pair is dependent on critical issues such as network topology and nodal degree.

Regarding the spectrum allocation sub-problem, the first-fit (FF) approach, a well-known and widely used spectrum allocation scheme, was selected. In a fixed-grid scenario, all wavelengths are initially numbered. When searching for available wavelengths, the first available wavelength is selected, i.e. a lower-numbered wavelength is always considered before a higher-numbered wavelength. By utilizing FF, it is possible to pack all in-use wavelengths towards the lower end of the wavelength space, and therefore longer continuous paths at the higher end of the wavelength space will remain available for future traffic requests. This scheme requires no global information, which guarantees small computational overhead, low complexity and small communication overhead.

Note that, since the main focus of this deliverable is on the static resource-allocation (RA) solutions, the way in which connections are ordered in the serving list plays an important role in the final outcome. To enhance the results in all cases under study, the simulated annealing (SimAn) meta-heuristic has been employed to find an appropriate ordering that yields a near-optimal result [39]. The SimAn procedure is detailed in section 3.4.

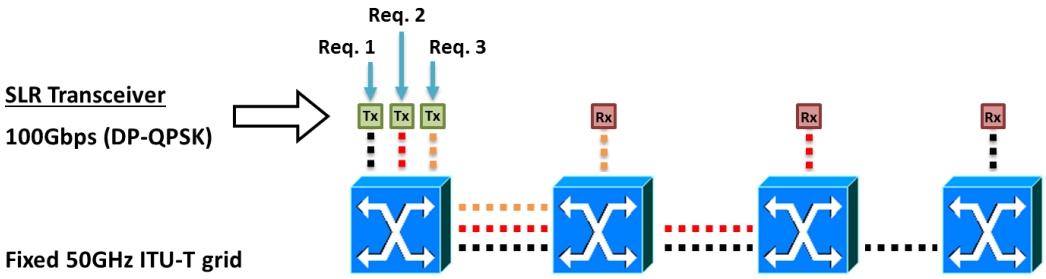


Figure 3.2 SLR transmission system over fixed ITU-T 50-GHz grid.

As a second benchmarking scenario, we analyse the MLR transmission system over flexi-grid. In this scenario an appropriately-sized portion of optical spectrum can be allocated to a connection request depending on the demand requirements. Thus, a lightpath can expand and contract according to the traffic volume and user request, which means that incoming traffic demands can be served in a spectrally efficient manner.

In a flexi-grid scenario, a number of contiguous spectrum slices, which have a finer granularity than the ITU-T 50-GHz grid (e.g. 12.5 GHz), is used to accommodate a connection. The continuity of these spectrum slices should be guaranteed in a similar manner as the wavelength continuity constraint is imposed on fixed-grid networks. This leads to the development of RMLSA algorithms [39], which, in the present study, consists of the previously mentioned FAR routing scheme and a modified version of the FF spectrum allocation algorithm. The new FF initially calculates the required spectrum for each incoming connection request regarding the traffic volume and the optical reach of the available modulation formats: DP-BPSK, DP-QPSK, DP-8QAM and DP-16QAM. Next, it searches for the necessary consecutive slots in ascending order of spectrum-slice index. The first set of spectral slices found fulfilling the requirements imposed by the connection request is selected. Similar to the SLR scenario, the SimAn meta-heuristic has also been included in the RA solution.

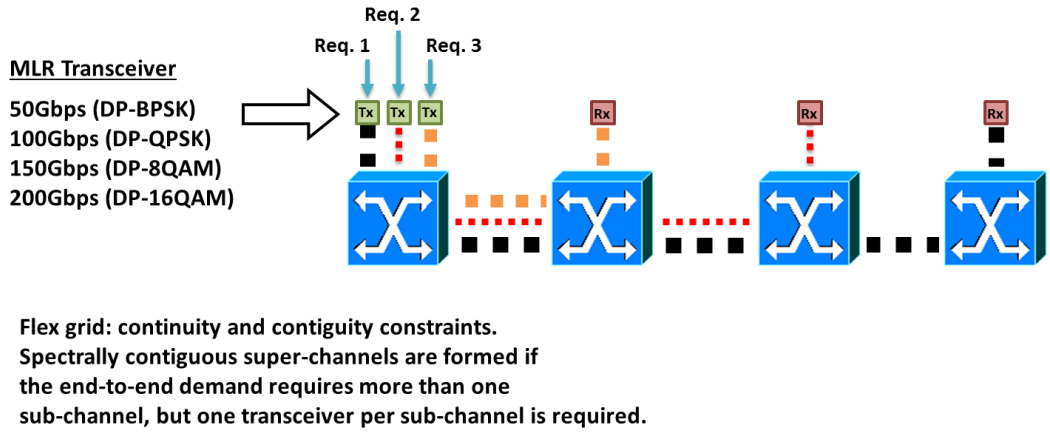


Figure 3.3 MLR transmission system over flexi-grid.

It is important to note that in a flexi-grid scenario, it is essential that a spectral portion should be allocated between adjacent connections to guaranty the quality of the signal at the receiver side. It is customary that the assigned spectrum portion between adjacent connections should be regarded as a multiple of the spectrum slice (e.g. 12.5GHz). The network-level performance is strongly dependent on the filter characteristics and the WDM frequency-grid granularity. However, a granularity of 6.25 GHz offers a good compromise between network performance and filter requirements for spectrum assignment to single-carrier signals, as demonstrated in [40].

3.4 ASTRON solutions

In the previous section, a set of well-known industrial solutions was presented. Another scenario would be for flexible optical networks to use super-channel transceivers, such as the transceiver solutions being investigated in the ASTRON project, to serve end-to-end connections (cf. Figure 3.4). Even though this scenario would dramatically increase the cost of the network on account of the more expensive transceivers, especially for small offered load values, it should bring a performance improvement for large offered load values due to the reduction in the inter-sub-channel guard bands. As demonstrated in [40], for sub-channel allocation within a super-channel, a significant performance improvement is observed when guard bands are made a multiple of 3.125 GHz as long as Nyquist-shaping filters with resolutions in the region of 1-1.2 GHz are used at the transmitter (finer filter resolutions and frequency slot granularities provide negligible performance improvement). The routing, modulation-level selection and spectrum allocation explained in section 3.3 can also be used here.

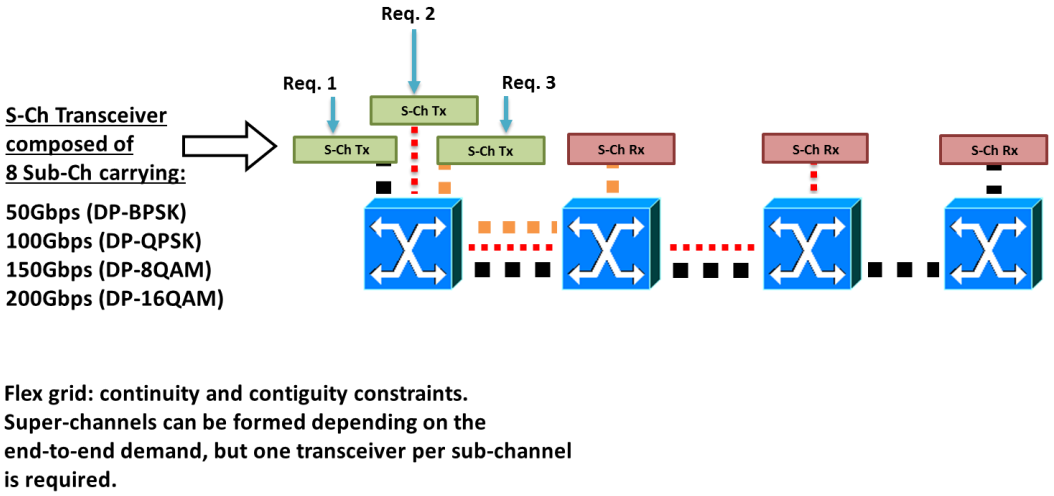


Figure 3.4 Non-grooming end-to-end connections supported by ASTRON super-channel transceivers.

To improve the spectrum utilization, in Figure 3.5 we present a modification of the end-to-end super-channel transmission scenario to allow all-optical traffic grooming at intermediate nodes enabled by the ROADMS with all-optical sub-channel A/D capability described in section 2.4. Therefore, a number of sub-channels can be dropped from or added to a super-channel, which should reduce the number of necessary super-channel transceivers especially in the case of networks with a large number of small traffic demands.

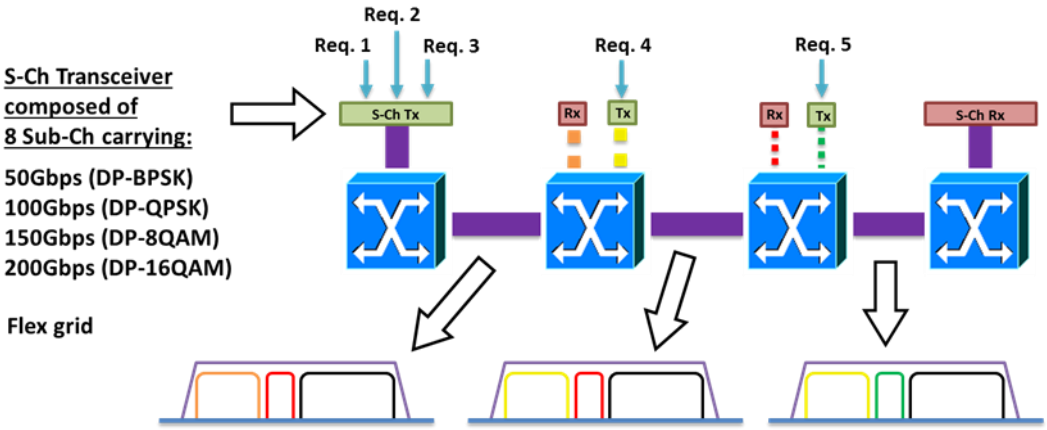


Figure 3.5 Super-channel transmission with all-optical traffic grooming at intermediate nodes enabled by ROADMS with all-optical sub-channel A/D capability.

To do the routing, modulation-level selection and spectrum allocation, we have developed an all-optical traffic grooming RMLSA (AOTG-RMLSA) algorithm. It is similar to the previously mentioned RA algorithms in that it uses the FAR routing algorithm to solve the routing problem and the modified version of FF (section 3.3) to select the modulation level and the spectrum allocation. The main difference between the AOTG-RMLSA algorithm and a conventional RMLSA algorithm is in steps 4 and 5 of the algorithm shown below, where the capability of all-optical traffic grooming at the network nodes is introduced.

AOTG-RMLSA algorithm [37]:

1. Let element R(s,d,b) be the connection request from source s to destination d, with bandwidth b. Put the elements in the serving list.
2. Sort serving list according to b in descending order (under the simulated annealing mega heuristic, make a copy of the serving list to be used as the initial solution). Set counter = 1.

3. Base element = serving list(counter). Compute k disjoint shortest paths to establish the base element.
4. For “Drop & Continue” take the following sub-steps (otherwise skip this step):
    I. For each computed path at step 3, create an empty list to register the possible elements R that can be groomed at the source node over the path. In the serving list find all unserved elements that meet the following conditions: s = same source as the base element, d = an intermediate node of the path. Register the elements in the path’s source grooming list.
    II. Select the path with the highest number of registered elements on the source grooming list. In case of a tie, select the shortest path in terms of distance.
    III. Calculate the modulation level and the number of sub-channels to serve the base element. Next, calculate the modulation level and the number of sub-channels for each of the elements in the source grooming list one by one.
    IV. Calculate the required spectrum for the super-channel formed as the juxtaposition of the sub-channels in the previous sub-step. Note that each super-channel has a maximum width limit determined by the utilized filter technology (e.g. 200 GHz for the HSR filter).
5. In the case of “Add & Drop” take the following sub-steps (otherwise skip this step):
    I. For each computed path at step 3, create an empty list to register the possible elements *R* that can be groomed at the source node over the path. In the serving list find all unserved elements that meet the following conditions: *s* = same source as base element, *d* = an intermediate node of the path. Register the elements in the path’s source grooming list.
    II. For each computed path at step 3, create an empty list to register the elements *R* that are groomed at the intermediate nodes. In the serving list find all unserved elements that meet the following conditions: *s* = *d* of registered element on the source grooming list of the path, *d* = same destination as the base element. Register the elements on the intermediate node grooming list.
    III. Select the path with the highest “number of registered elements on the source grooming list + number of registered elements on the intermediate node grooming list”. In case of a tie, select the shortest path in terms of distance.
    IV. Calculate the modulation level and the number of sub-channels to serve the base element. Next, calculate the modulation level and the number of sub-channels for each of the elements on the source grooming list and the intermediate node grooming list one by one.
    V. Calculate the required spectrum for the super-channel formed as the juxtaposition of the sub-channels in the previous sub-step. Note that each super-channel has a maximum width limit determined by the utilized filter technology (e.g. 200 GHz for the HSR filter).
6. Find the first sufficient spectrum portion for the super-channel so that it complies with the spectrum continuity and contiguity constraints.
7. Mark all served elements on the serving list as served connection requests. Counter++ and go to step 3 while counter ≠ size of serving list.
8. If there still exist unserved elements on the serving list, consider them as blocked connections.

9. Under the simulated annealing meta-heuristic, re-arrange the copy of the serving list according to the simulated annealing rules, set counter = 1 and go to step 3. Repeat for a set number of iterations.

In line with the discussion in section 3.3, step 9 involves the utilization of the simulated annealing (SimAn) meta-heuristic in the RA solution. Under the SimAn, the algorithm starts with the initial ordering of the serving list resulting from step 2 and calculates its cost (viewed as "energy" in SimAn setting) by serving the connections one by one, using the part of the algorithm between step 3 and 8 ("fitness function"). For a particular ordering (R_1, R_2, …, R_M) of *M* demands, we define its neighbour as the ordering where R_i is interchanged with R_j. To generate a random neighbour, R_i and R_j are pivoted uniformly among the *M* demands. This random neighbour creation procedure and the fitness function are used in a typical SimAn iterative procedure to minimize an optimization objective. Here, the objective is to minimize the total cost of ownership, which is described in more detail in the next section.

3.5 Total cost of ownership analysis

To evaluate the performance of the ASTRON project transceiver solutions, we carry out a total cost of ownership (TCO) analysis. Based on [41] and [42], the TCO comprises two main expenditures: transceiver cost and network node cost, which can be extracted from a network planning study. These expenditures can be easily calculated by multiplying the number of network components (transceiver and optical cross connect elements) according to the cost model presented in chapter 2.

As a first step, resources (such as transceivers –TRx– and spectrum) are appropriately assigned to traffic demands by means of a routing, modulation level and spectrum allocation algorithm (e.g. the AOTG-RMLSA algorithm presented in section 3.4 for the ASTRON transceiver solutions) in a network planning scenario, such that blocking-free connection establishment can be guaranteed while minimizing the spectral occupancy. Subsequently, the total equipment cost (TEC) is calculated, for a number *N* of elements (TRx and ROADMs) and their corresponding unit costs *C*, according to the equation:

$$TEC = N_{TRx} \times C_{TRx} + N_{ROADM} \times C_{ROADM}.$$

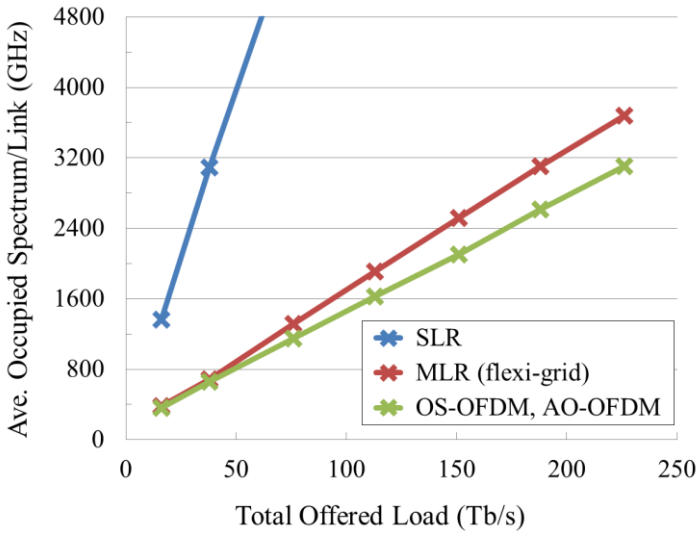


Figure 3.6 Spectrum occupancy vs. total offered load [43].

As an outcome of the network planning study, Figure 3.6 shows the average occupied spectrum per link versus total offered load to the network for the SLR, MLR and two super-channel transmission scenarios. It is observed that the spectral gain obtained by the super-channel transceiver solutions when used in combination with ROADMs with all-optical sub-channel A/D capability increases almost linearly with the offered load. The reason behind this is that for higher loads the number of groomed

sub-channels per super-channel increases, and therefore the spectrum savings due to the elimination of guard bands between sub-channels becomes more significant. For the highest offered load in the graph (226 Tb/s) this saving is ~15%.

In Figure 3.7 we show a comparison of the total transceiver cost in the network for the benchmarking cases (SLR, MLR) and the super-channel transceivers under consideration in the ASTRON project: OS-OFDM (which has the same cost as the NFDM/eOFDM super-channel transceivers), AO-OFDM (with DSP), and NWDM with optical filtering (incorporating one N×1 HSR filter or two 1×1 HSR filters).

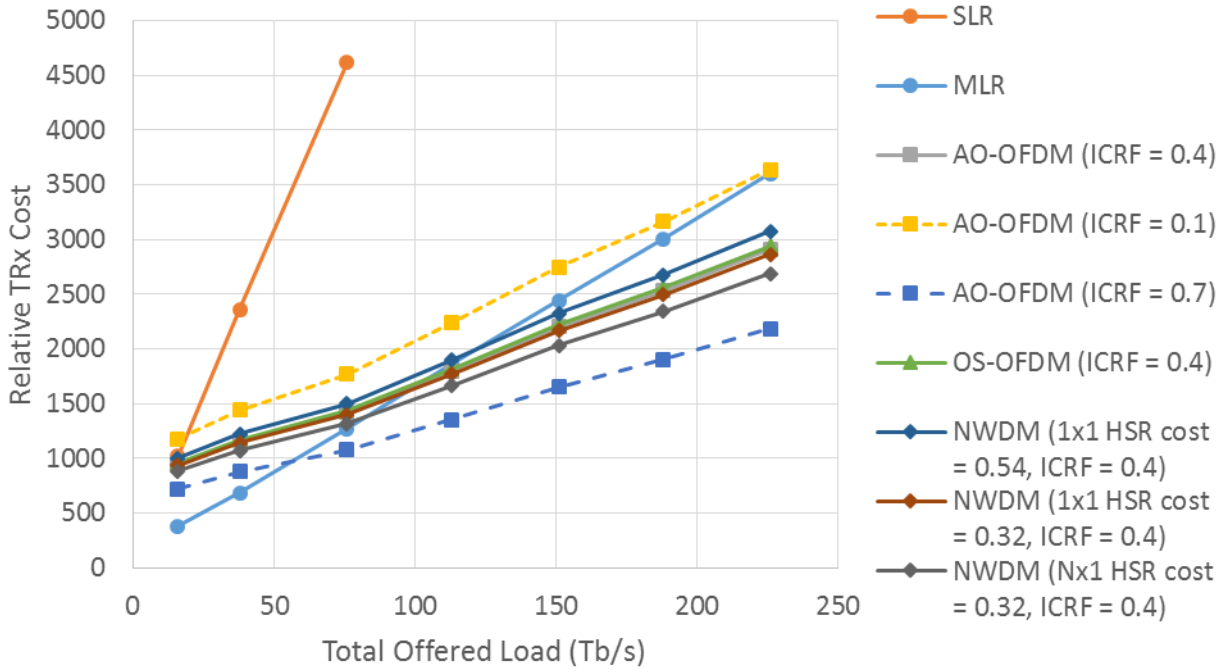


Figure 3.7 Relative transceiver (TRx) cost as a function of the total offered load to the network. Solid line: single-carrier solutions and super-channel solutions with ICRF = 0.4. Dashed line (short dashes): ICRF = 0.1. Dashed line (long dashes): ICRF = 0.7.

MLR is the best solution for low total offered loads because it exhibits a good network performance (as shown in Figure 3.6) and is the most cost-effective solution. However, MLR becomes more expensive than any of the super-channel solutions (with ICRF = 0.4) when the load increases above 125 Tb/s, and it is about 30% more expensive than the super-channel solutions when the load is 226 Tb/s. All the super-channel solutions (with ICRF = 0.4) present a similar transceiver cost behavior, with the AO-OFDM and OS-OFDM showing the best performance unless the cost of the HSR filter used in the NWDM transceivers can be brought down to 0.32 (current cost of a 1×9 WSS). In particular, the solution based on the single N×1 HSR filter shows a 7.5% cost reduction with respect to the AO-OFDM solution.

Furthermore, to evaluate the impact of component integration on the total transceiver cost, we varied the ICRF between 0.1 and 0.7 for the AO-OFDM solution (the results can be applied to all other transceiver solutions). For large loads (226 Tb/s) we observed a cost reduction of ~25% when the ICRF is increased from 0.4 to 0.7. This is therefore the most important parameter in effectively bringing down the total transceiver cost, which, as we will see later, is the main contributor to the total network equipment cost.

The results of the TEC analysis are presented in Figure 3.8 and Figure 3.9. In Figure 3.8 we plotted the total cost for SLR, MLR and several super-channel transceiver scenarios (assuming an ICRF = 0.4) in a network with colourless, directionless R&S ROADMs. The SLR and MLR scenarios use conventional ROADMS, whereas the super-channel transmission scenarios have built-in all-optical sub-channel add/drop capability provided by two-tier HSR-based (for non-overlapping sub-channels, such as in the

OS-OFDM and NWDM cases) and TIDE-based (for overlapping sub-channels, such as in the case of AO-OFDM) A/D stages, as described in section 2.4.2. In the study, we assumed two relative costs for the HSR filter/WSS: 0.54 (current cost, shown in solid line) and 0.32 (1×9 WSS cost, shown in dashed line). The total equipment cost evolution is very similar to that of the transceiver cost, which indicates that the transceivers are the main source of expenditure. This is so because, while thousands of single-carrier transceivers are required to establish the connections for large loads in the SLR case, and hundreds of super-channel transceivers (with a cost 5-6 times larger than that of a single-carrier transceiver) are employed in the super-channel transmission solutions, only 51 ROADMs (with average degree D = 2.9 and relative cost of 5.80 for the conventional ROADM, and 6.53 and 7.36 for the ROADM with M = 1 all-optical sub-channel A/D cards based on the HSR filter or the TIDE processor, respectively) are needed, regardless of the offered load to the network. Therefore, as happened in Figure 3.7, the MLR case is less expensive than the super-channel solutions for low loads. Regarding OS-OFDM, AO-OFDM and NWDM, they show a very similar performance, especially for low loads, but their curves diverge slowly (in particular NWDM) as the load increases, with AO-OFDM proving to be slightly more cost-effective (~1% and 5% less costly than OS-OFDM and NWDM, respectively). However, if the relative cost of the optical filtering technology (HSR and WSS) could be brought down to 0.32, NWDM would become the most inexpensive solution, with savings amounting to ~7-8% with respect to AO-OFDM and OS-OFDM when N×1 HSR filters are employed at the transmitters.

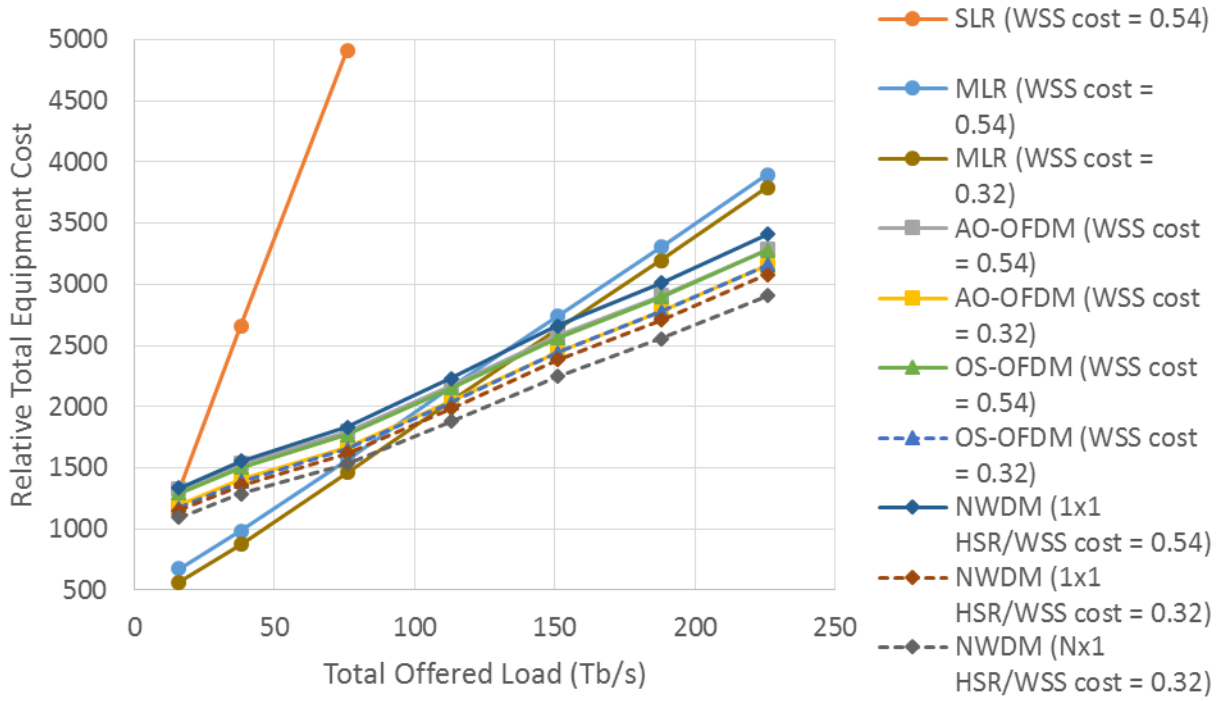


Figure 3.8 Total equipment cost as a function of the total offered load for a network with colourless, directionless R&S ROADM. For the super-channel transceivers we considered ROADMs with all-optical sub-channel A/D capability based on HSR filters (for non-overlapping sub-channels, i.e. OS-OFDM and NWDM) and TIDE processors (for overlapping sub-channels, i.e. AO-OFDM). Solid lines: HSR/WSS cost = 0.54. Dashed lines: HSR/WSS cost = 0.32. ICRF = 0.4.

Figure 3.9 shows total cost for SLR, MLR and several super-channel transceiver scenarios (assuming an ICRF = 0.4) in a network with colourless, contentionless R&S ROADMs. The results are almost identical (but slightly shifted down) to those shown for the networks based on colourless, directionless ROADMs due to the fact that the transceiver cost is dominant in the total equipment cost calculation for the reasons pointed out in the previous paragraph.

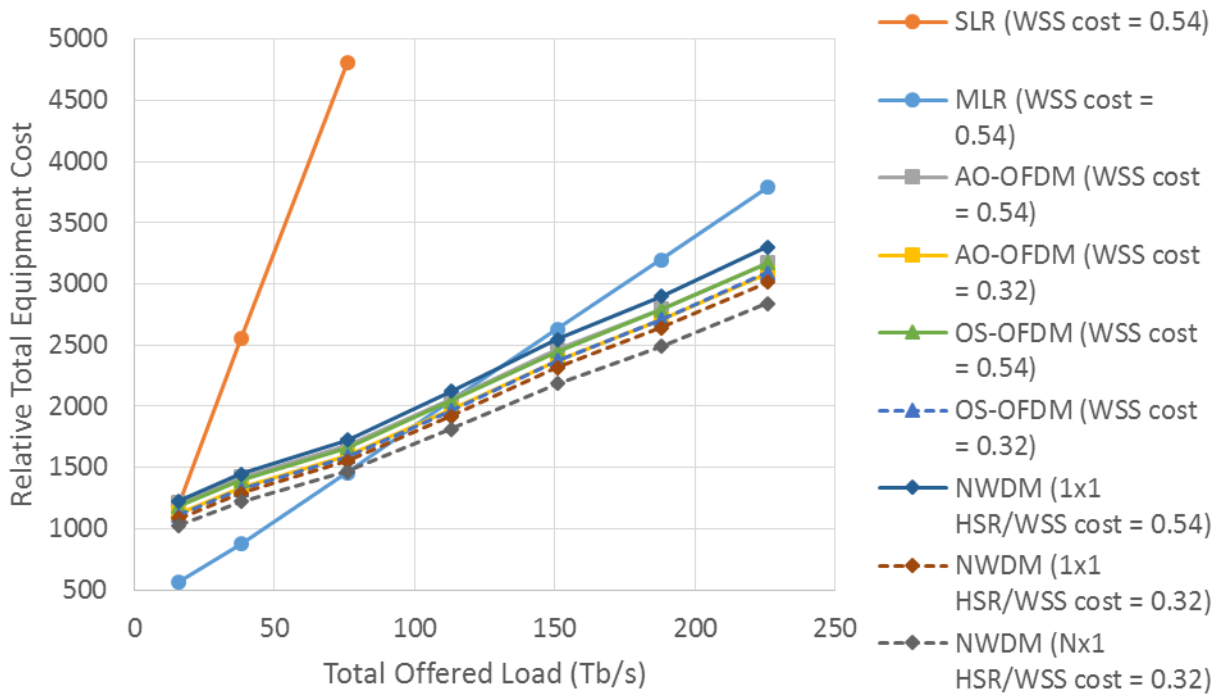


Figure 3.9 Total equipment cost as a function of the total offered load for a network with colourless, contentionless R&S ROADM. For the super-channel transceivers we considered ROADMs with all-optical sub-channel A/D capability based on HSR filters (for non-overlapping sub-channels, i.e. OS-OFDM and NWDM) and TIDE processors (for overlapping sub-channels, i.e. AO-OFDM). Solid lines: HSR/WSS cost = 0.54. Dashed lines: HSR/WSS cost = 0.32. ICRF = 0.4.

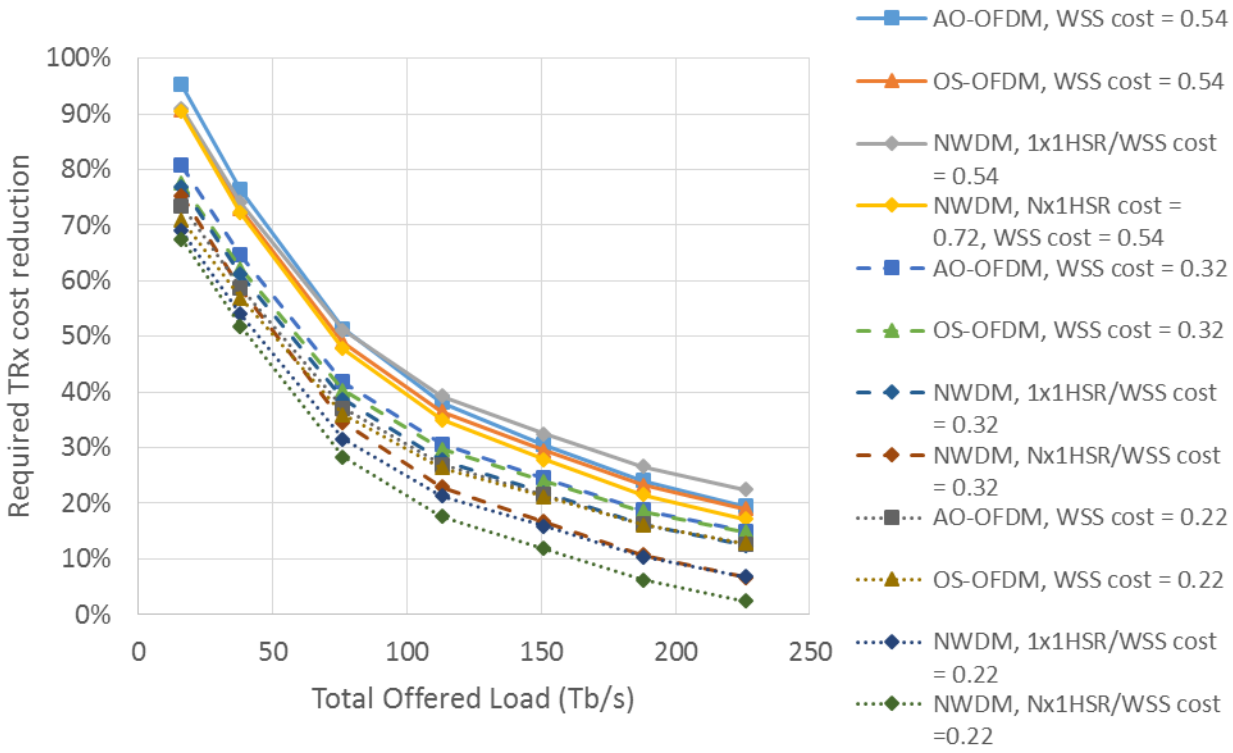


Figure 3.10 Super-channel transceiver cost reduction required to achieve 30% TEC savings with respect to the MLR scenario as a function of the total offered load for a network with colourless, directionless R&S ROADM. We considered ROADMs with all-optical sub-channel A/D capability based on HSR filters (for non-overlapping sub-channels, i.e. OS-OFDM and NWDM) and TIDE processors (for overlapping sub-channels, i.e. AO-OFDM). Solid lines: HSR/WSS cost = 0.54. Dashed lines: HSR/WSS cost = 0.32. Dotted lines: HSR/WSS cost = 0.22. ICRF = 0.4.

To conclude the TEC analysis, we plotted in Figure 3.10 the super-channel transceiver cost reduction required to achieve 30% TEC savings with respect to the MLR scenario as a function of the total offered load to the France Telecom national network, assuming colourless, directionless R&S ROADMs at the nodes. We considered ROADMs with all-optical sub-channel A/D capability based on HSR filters (for non-overlapping sub-channels, i.e. OS-OFDM and NWDM) and TIDE processors (for overlapping sub-channels, i.e. AO-OFDM) with different 1 × 20 WSS costs: 0.54 (current cost), 0.32 (current 1 × 9 WSS cost), and 0.22. For the super-channel transceivers, we assumed an integration reduction factor equal to 0.4. We observed that, with WSS cost = 0.54, the NWDM transceiver solution with N × 1 HSR filters (with cost = 0.72) provides the best performance, with a transceiver cost reduction of only 17% (in comparison with 19% for AO-OFDM and OS-OFDM for total load = 226 Tb/s) required to reach 30% TEC savings, with the caveat that the development of the N × 1 HSR filter is still ongoing and therefore this technology is not currently available. NWDM with 1 × 1 HSR filter with cost = 0.54 outperforms AO-OFDM for low loads, but it becomes the worst-performing solution for higher loads. This is because the ROADM architecture for AO-OFDM uses TIDE processors instead of HSR filters, which increases the TEC for AO-OFDM for low loads. As observed in Figure 3.10 the use of one or another sub-channel A/D technology has no impact on the required transceiver cost reduction for large loads, since the transceiver cost is the dominant source of expenditure.

When the 1 × 20 WSS/HSR filter cost is decreased to 0.32 and 0.22, the optical-filter-based transceiver solutions lead to a required transceiver cost reduction for large loads of just 12% and 7% (when they use two 1 × 1 HSR filters) or 7% and 2% (when they use one N × 1 HSR filter), respectively. The AO-OFDM and OS-OFDM solutions would require in this case a reduction of 15% and 13% respectively.

When it comes to the power consumption, in Figure 3.11 we show the annual energy consumption of all the required transceivers in the France Telecom national network as a function of the total offered load for different transceiver implementations. Regarding the ASTRON transceivers, two OS-OFDM cases are considered, one in which the DSP power consumption assumes the value of 24W per sub-channel, as estimated in section 2.2.2, and another one with a more conservative value (30W per sub-channel). Additionally, we considered the AO-OFDM solution described in section 2.2.1.2.

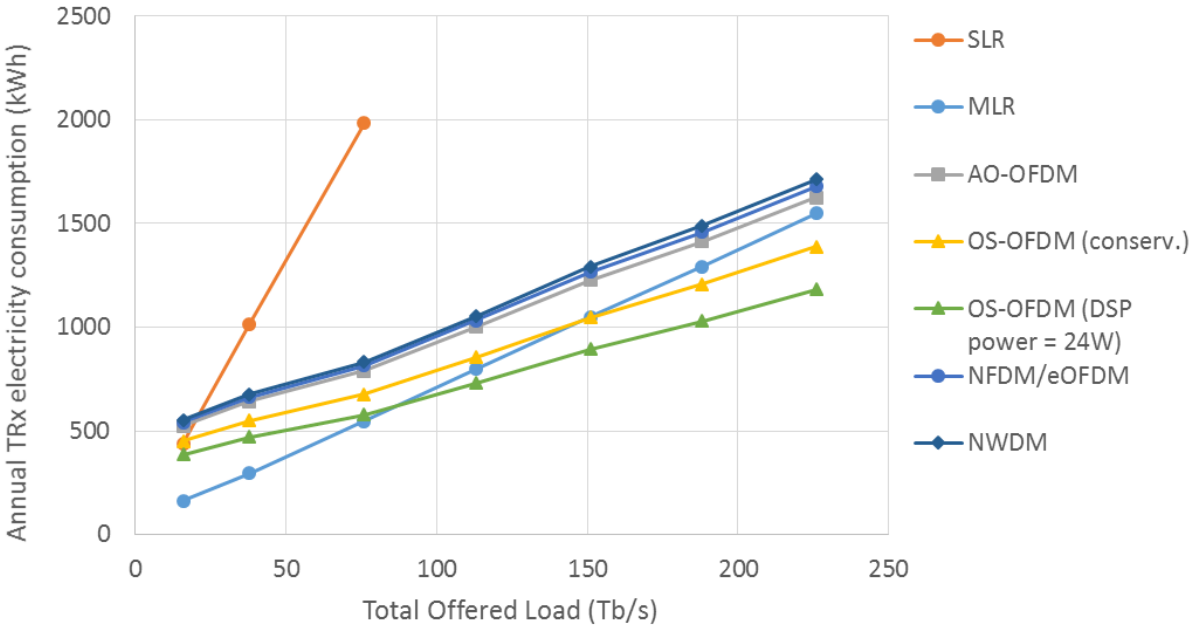


Figure 3.11 Annual energy consumption of all the required transceivers in the France Telecom national network as a function of the total offered load.

The MLR solution, utilising single-carrier transceivers, is less power-consuming than NWDM with optical filtering (based on the 1×1 HSR filter), NFDM/eOFDM/conventional AO-OFDM and the ASTRON

AO-OFDM solution, the latter performing slightly better than the previous two. OS-OFDM outperforms MLR for total offered loads greater than 150 Tb/s and 90 Tb/s when the DSP power consumption per sub-channel is equal to 30W and 24W, respectively. For 226 Tb/s, they provide an energy consumption reduction of 8% and 21% with respect to MLR. In Figure 3.12 we converted the energy consumption into electricity cost by assuming a cost of 0.12€/kWh, according to the average price of electricity for industrial use in EU-28 during the 2nd half of 2014, reported by Eurostat in August 2015.

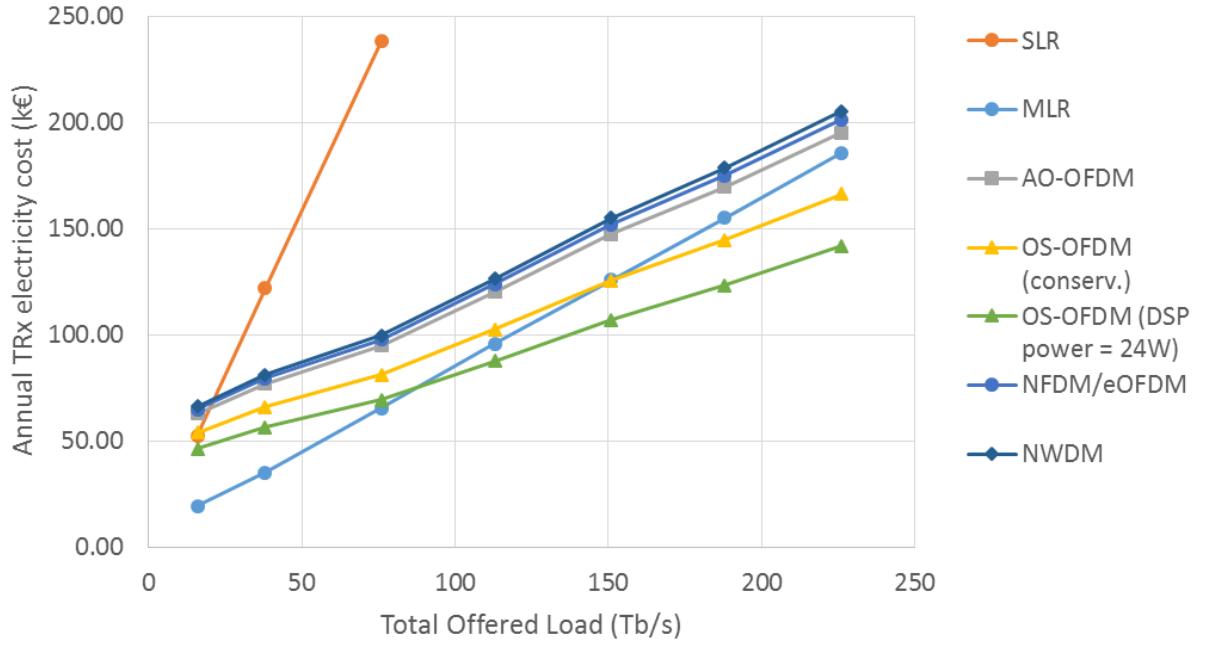


Figure 3.12 Annual electricity cost of all the required transceivers in the France Telecom national network as a function of the total offered load.

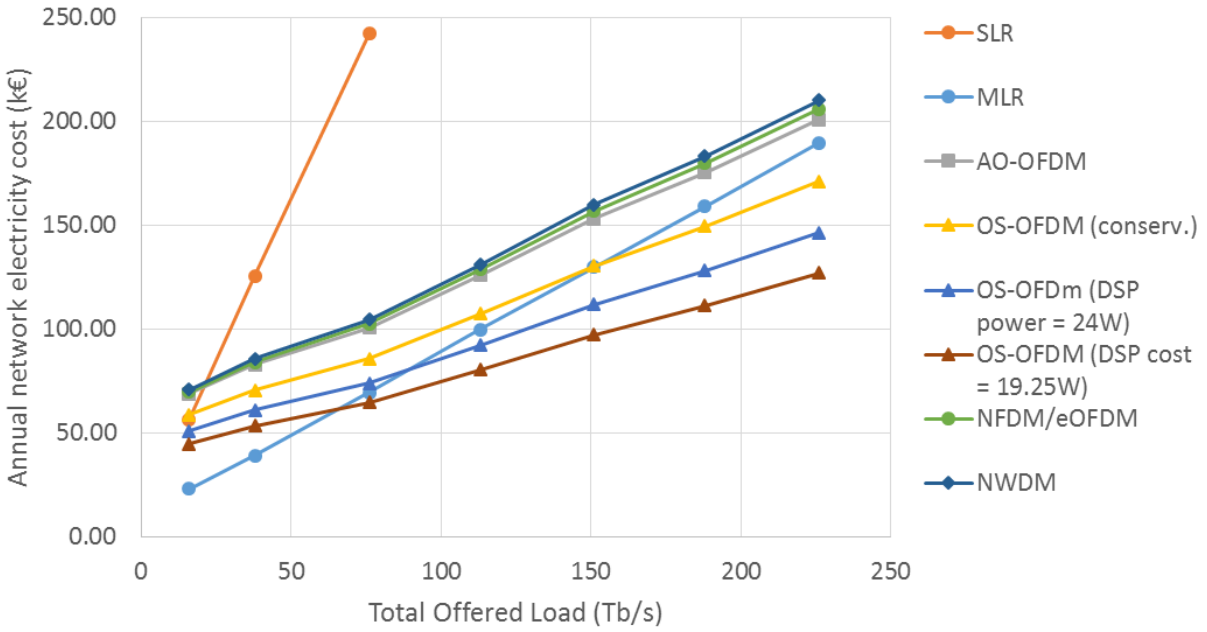


Figure 3.13 Annual electricity cost of all the required network equipment (TRx and colourless, directionless ROADMs) in the France Telecom national network as a function of the total offered load. ROADM PRF = 0.1.

Figure 3.13 and Figure 3.14, in turn, show the annual electricity cost of transceivers and ROADMs (both colourless, directionless and colourless, contentionless, with power reduction factor (PRF) equal to 0.1, cf. section 2.4) in the network. As pointed out above, due to the low number of ROADMs, especially

for larger loads, the transceivers are dominant, which explains the similarities between Figure 3.12, Figure 3.13 and Figure 3.14.

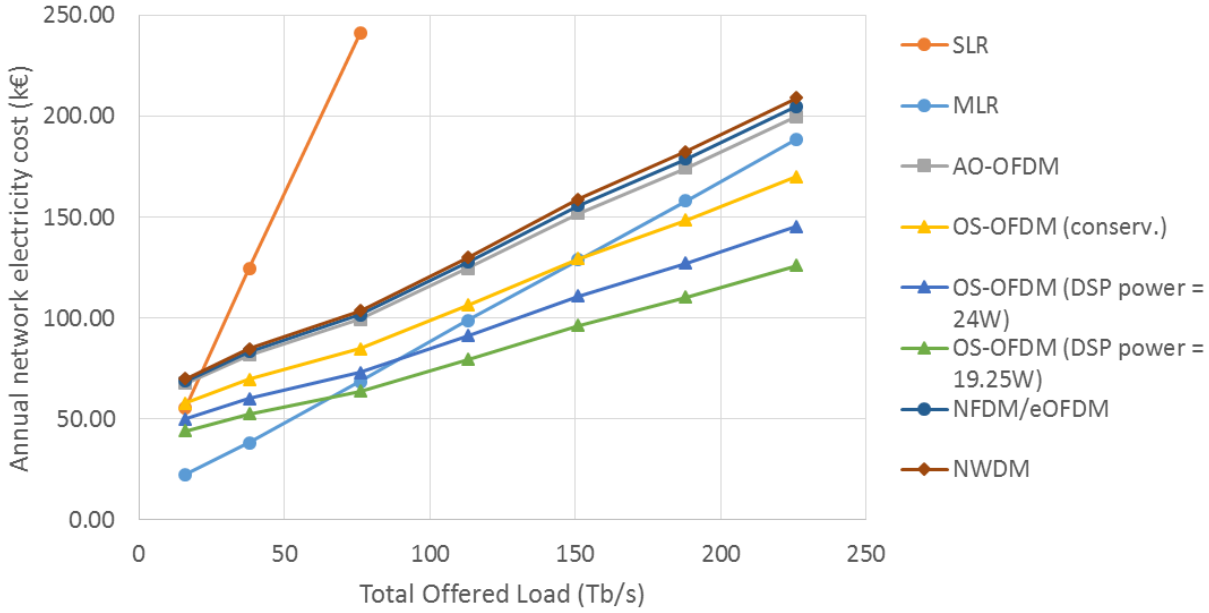


Figure 3.14 Annual electricity cost of all the required network equipment (TRx and colourless, contentionless ROADMs) in the France Telecom national network as a function of the total offered load. ROADM PRF = 0.1.

To study the influence of the PRF on the network power consumption, we plotted in Figure 3.15 the annual electricity cost of the network assuming colourless, directionless ROADMs with PRF equal to 0.1 and 0.4. We carried out this study only for the MLR and OS-OFDM solutions, considering DSP power consumptions per sub-channel equal to 30W, 24W and 19.25W (50% of the single-carrier transceiver DSP power consumption). The results indicate that the PRF has a minimal effect on the total power consumption and that it the DSP power that needs to be reduced if a significant electricity cost reduction wants to be achieved.

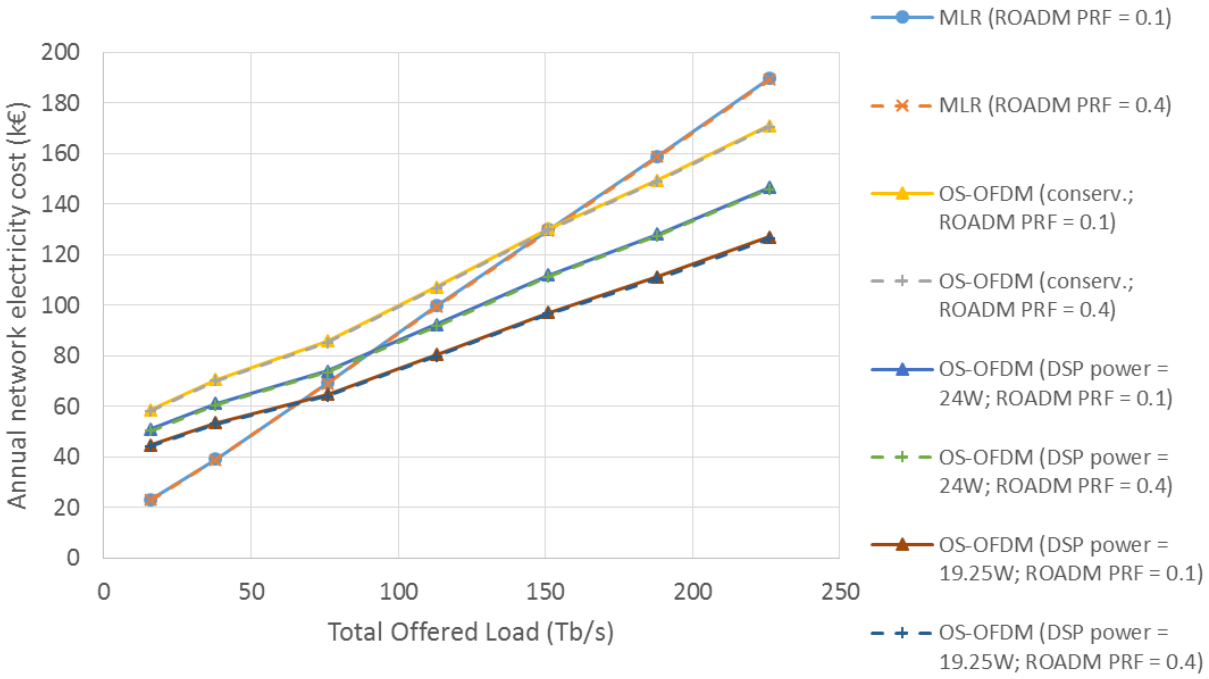


Figure 3.15 Annual electricity cost of all the required network equipment (TRx and colourless, directionless ROADMs) in the France Telecom national network as a function of the total offered load for two ROADM PRF: 0.1 (solid) and 0.4 (dashed).

Finally, in Table 3.1 we present the cumulative electricity cost over the time period corresponding to the offered loads shown on the x-axis in Figure 3.12-Figure 3.15. Only the OS-OFDM solutions with DSP power equal to 24W and 19.25W perform better than MLR (-6% and -18%, respectively, for the colourless, directionless ROADM architecture), with the OS-OFDM solution with DSP power equal to 30W showing an electricity cost increase of 9% and the AO-OFDM solution an increase of 28%.

Table 3.1 Electricity cost (in k€) of all the required network equipment (TRx and ROADMs) in the France Telecom national network over the period represented in Figure 3.15 for PRF equal to 0.1 and two ROADM architectures: colourless, directionless (CD) and colourless, contentionless (CC).

ROADM	MLR	NFDM/ eOFDM	NWDM	AO-OFDM	OS-OFDM (DSP power = 30W)	OS-OFDM (DSP power = 24W)	OS-OFDM (DSP power = 19.25W)
CD	710	927	946	907	774	665	579
CC	707	921	940	900	768	659	572

However, if we consider the period starting from the moment when MLR fails to provide a hardware cost benefit (~113 Tb/s), according to Figure 3.8, the cumulative electricity cost for the MLR and OS-OFDM would be:

MLR: 578 k€

OS-OFDM (DSP power = 30W): 558 k€

OS-OFDM (DSP power = 24W): 479 k€

OS-OFDM (DSP power = 19.25W): 416 k€

which translates into cost reductions amounting to 3%, 17% and 28%, respectively.

4. Conclusions

In this report, we presented the cost and power consumption reference model for the ASTRON project and carried out a techno-economic analysis to evaluate the advantages of the proposed transceiver solutions in terms of total equipment cost and energy consumption over a representative European national network.

In chapter 2, we showed the results of the cost and power consumption estimation of (a) the super-channel transceivers being developed in the ASTRON project, as well as benchmarking single-carrier and multi-carrier transceivers, and (b) conventional ROADMs for end-to-end single-carrier/super-channel transmission and ROADMs with the capability of all-optically adding and dropping sub-channels from Nyquist WDM and OFDM super-channels. Regarding the ASTRON super-channel transceivers, we showed that monolithic integration alone cannot ensure their financial viability, since our results indicate that as the number of IQ modulators in a PIC increases, so does the area per IQ modulator, which leads to far fewer PICs per wafer, lower yields and, ultimately, a cost increase. However, monolithic integration (or the more advanced heterogeneous integration) does enable the transfer of an increasing number of connections and functions from the backend to the frontend, thereby bringing advantages in terms of performance and compactness, as well as packaging, assembly and testing cost savings, which nowadays dominate the cost of optical components. Further improvement of monolithic/heterogeneous integration, fibre-coupling techniques based on passive processes, along with integrated diagnostic devices for in-situ testing will yield additional benefits in terms of cost and reliability.

The ASIC module, which builds in the ADCs/DACs, the DSP and the SD-FEC modules, also accounts for a large share of the transceiver cost, this figure ranging from 20% to 50% depending on the cost reduction afforded by (a) integration and packaging, (b) the number of integrated sub-channels and (c) whether or not the systems vendors have in-house DSP chip development capability. Smaller CMOS process sizes, such as 20 or 16nm, can result in cost and power consumption savings with a significant impact on the final transceiver cost. Furthermore, the ASIC accounts for more than 70% of the power consumption of the transceiver, and therefore the use of more efficient semiconductor technologies and less complex DSP algorithms can be extremely beneficial. To gain a deeper insight into this issue, the complexity of several linear- and nonlinear-impairment equalization algorithms was evaluated. We demonstrated that the ASTRON-project filter-bank based OS-OFDM super-channel solution can provide around 44% complexity reduction in comparison with a conventional transceiver, while ensuring a good transmission performance, as reported in e.g. D2.4. The transmission reach can be further improved by making use of nonlinear equalization techniques such as digital back-propagation or inverse Volterra series. Our results showed that the complexity of DBP-SSF_1 and Volterra is within practical limits, but DBP-SSF_3 is impractical since its power consumption and ASIC area are prohibitively high.

Finally, in chapter 3, we reported on the results of a techno-economic analysis of the ASTRON-project super-channel transceiver implementations conducted over the France Telecom national network. We observed that the ASTRON solutions, when used in combination with ROADMs with all-optical sub-channel A/D capability, offered savings in terms of spectrum usage and total equipment cost amounting to, respectively, 15% and 30% (with respect to MLR) for large total offered loads (more than 150 Tb/s). An additional cost reduction of up to 25% can be achieved through further integration and packaging transceiver cost reductions. As for the power consumption, the use of the filter-bank approach in the ASTRON super-channel transceiver solutions results in energy savings between 8% and 30% (with respect to MLR) when the filter-bank based DSP power consumption decreases by a percentage ranging between 22% and 50% with respect to the DSP power consumption of a conventional single-carrier transceiver.

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