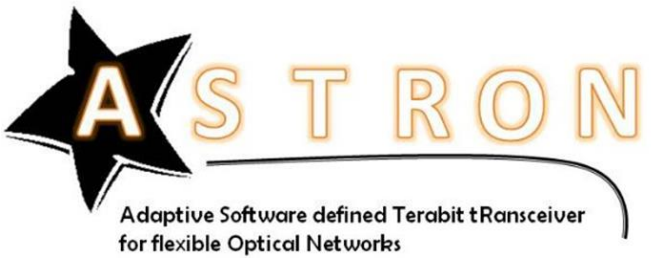

ADAPTIVE SOFTWARE DEFINED TERABIT TRANSCEIVER FOR FLEXIBLE OPTICAL NETWORKS

FP7-ICT-GA 318714

SPECIFIC TARGETED RESEARCH PROJECT (STREP) INFORMATION & COMMUNICATION TECHNOLOGIES (ICT)

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Adaptive Software Defined Terabit Transceiver For Flexible Optical Networks

At A Glance

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Project Partners

- OPTRONICS TECHNOLOGIES SA (OPTRONICS), EL
- FINISAR ISRAEL LTD (FINISAR), IL
- FRAUNHOFER-GESELLSCHAFT ZUR FOERDERUNG DER ANGEWANDTEN FORSCHUNG E.V (HHI), DE
- RESEARCH AND EDUCATION LABORATORY IN INFORMATION TECHNOLOGIES (AIT), EL
- UNIVERSITY COLLEGE LONDON (UCL), UK
- UNIVERSITA DEGLI STUDI ROMA TRE (RM3), IT
- ALBIS OPTOELECTRONICS AG (ALBIS), CH
- AIFOTEC AG (AIFOTEC)
- ERICSSON TELECOMUNICAZIONI (TEI), IT
- NATIONAL INSTITUTE OF INFORMATION AND COMMUNICATIONS TECHNOLOGY (NICT), JP
- OPTOSCRIBE LTD (OPTOSCRIBE), UK
- TECHNION - ISRAEL INSTITUTE OF TECHNOLOGY (TECHNION), IL

Vision and Aim

ASTRON project aimed at the design and development of an integrated optical transceiver (Tx/Rx) that enables the wide and cost-efficient deployment of flexible core and access networks.

The main features of the Tx/Rx are the following:

- Reconfigurable bandwidth allocation using either Optical OFDM or Nyquist WDM technology
- Programmable modulation formats
- Programmable data rate
- Programmable FEC (offering tunability of the ratio of the actual payload to the FEC)
- Energy-efficiency by incorporating state-of-art digital, analog, mixed-signal and optical components into an integrated platform
- Design for Manufacturability using components that can be easily produced at low cost embedded into a compatible package

The implementation of such a system provide a low-power and low-cost alternative to the use of expensive and power hungry transceivers made from discrete components. The transmitter and receiver modules are designed to be packaged into a small form factor module in order to be compatible with the current network devices. During the ASTRON project the design and the development of compact and scalable photonic integrated components as well as all the necessary electronic circuits and state of the art algorithms to drive and control the optical devices were realized. These devices are capable of generating and receiving advanced-modulation-formats (QPSK, 16 QAM) encoded optical signals for high capacity (beyond 1Tb/s) networks. The unique features of the ASTRON architecture allow the transmitter to dynamically support different transmission technologies (optical OFDM or Nyquist WDM) and due to the advanced software-defined signal processing, the proposed system supports different data rates providing flexibility and efficiency [1].

Main Objectives

1. Design and fabrication of all optical IDFT/DFT AWG-based structures
    a. The Arrayed Waveguide Grating (AWG) is the core piece in both basic components of the ASTRON transceiver, transmitter and receiver. The device has 8 inputs and output ports and a free spectral range of FSR=200 GHz.
    b. This AWG is monolithically integrated on the transmitter and receiver planar silica (glass) motherboard together with an optical 1x8 power splitter/combiner.
2. Development and fabrication of InP-based IQ Mach-Zehnder Modulator chips
    a. Monolithic InP-based 1.55 µm 4-channel (Quad) -IQ Mach-Zehnder modulator (MZM) Photonic Integrated Circuits (PIC) are designed and fabricated in ASTRON for hybrid assembly onto novel planar passive optical transmitter glass boards.
    b. To fabricate the fully integrated planar hybrid transmitter lightwave circuit and to achieve the target maximum device throughput of 1.12 Tb/s, two 4-channel IQ MZM PICs are assembled.
3. Design and development of an integrated multi-channel transmitter (Tx) module
    a. The fully integrated transmitter consists of the active InP MZMIQ chips, the passive 1x8 optical power splitter, and the 8x8 AWG structure (enabling the iDFT functionality).
    b. The electrical DC/RF chip-to-board connections as well as the routing of the resulting large number of electrical DC/RF tracks on the optical glass board are addressed in order to achieve the specified aggregate terabit transmitter capacity.
4. Design and development of an integrated optical coherent receiver (Rx) module
    a. The ASTRON Rx module consists of an 8x8 AWG-based waveguide structure with DFT functionality, optical 90° hybrids, 25 GHz RF traces as well as supporting structures for hybridization to high speed (≥25 GHz) balanced photodetector arrays.
    b. All the optical and electrical functions are integrated into/onto a passive silica (glass) receiver motherboard.
5. Development of a hybrid integration platform
    a. Development of a hybrid “monolithic-on-hybrid” or so-called PIC-on-Glass (POG) integration approach which relies on the hybrid assembly of active InP devices onto a a passive planar Rx/Tx glass motherboard. In case of the Tx a horizontal optical coupling scheme is used by applying flip-chip bonding technology, while the light is coupled vertically in the Rx by using a suitable mirror integrated in the glass board.
    b. Separate development of the active and passive Tx/Rx building blocks with respect to the specific needs of the hybrid POG approach.
6. Development of novel software defined Signal Processing modules and DSP techniques
    a. Software defined signal processing modules enable the transceiver to be flexible in terms of modulation format, bit rates and bandwidth allocation
    b. DSP techniques are developed for the electronic mitigation of impairments
7. Performance evaluation of the ASTRON transceiver in a terabit-capacity optical testbed.

Technical Approach and role of partners

A hybrid transmitter (Tx) Planar Lightwave Circuit (PLC) and a hybrid receiver (Rx) PLC are the core components of the ASTRON transceiver (Fig. 1). The fabrication of both components is based on the hybrid coupling of monolithic active InP PICs (Mach-Zehnder modulators, photodetectors) with a passive optical silica-based (glass) motherboard. . Thereby cost-effectiveness, high yield fabrication, small footprint, low power consumption and device scaling is achieved. The photonic integration platform developed in ASTRON uses a "monolithic-on-hybrid" technology in order to integrate the active and passive building blocks to form a complete transmitter-receiver system. The Tx PLC integrates an optical 8-port Arrayed Waveguide Grating (AWG) which optically implements the Inverse Discrete Fourier Transform (IDFT), two 4-channel (Quad) InP-based In Phase-Quadrature (IQ) modulators arrays and a passive optical power splitter (Figure 2, Figure 3). In order to have OFDM or Nyquist WDM data flow, the necessary adaptation is possible to be implemented in the Radio Frequency (RF) domain. In this way the switching between the two technologies depends on the driving conditions of the IQ-modulators [2].

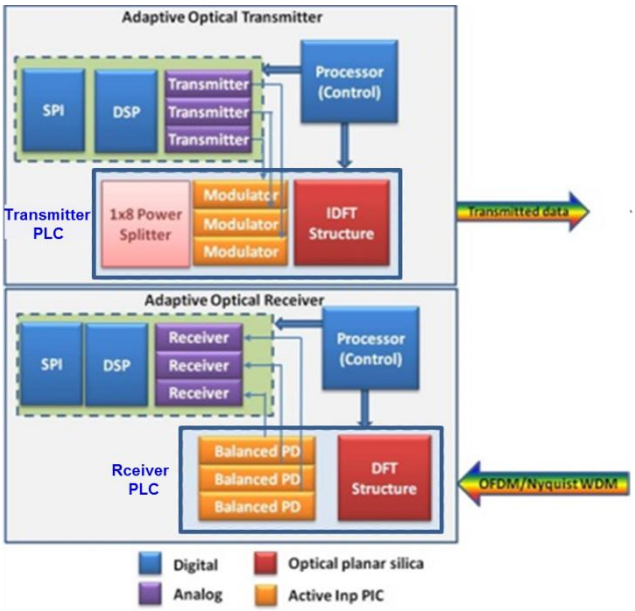


Figure 1: Architecture of the adaptive software defined optical transceiver

The Rx PLC consists of a similar 8-port AWG structure that implements the Discrete Fourier Transform (DFT) in order to decode the incoming signals and an array of 90° hybrids followed by balanced Photo-Detectors (PD), Figure 4.

The active InP elements enable the generation, modulation and detection of 200 Gsymbol/s optical signals and are assembled onto the passive optical silica motherboards.

The optical silica motherboards do not integrate only the passive optical IDFT and DFT AWG structures, splitters/combiners, mirrors, and 90° hybrids, but also electrical co-planar radio frequency (RF) transmission lines and AuSn solder pads for flip-chip bonding.

The beneficiaries that form the core of the technology development within ASTRON are HHI, ALBIS, AIFOTEC, OPTOSCRIBE and FINISAR. In more detail, HHI fabricates the monolithic large scale quad IQ-MZM PICs on InP and carries out research for **developing high-yield monolithic modulator arrays/PICs**. On the other hand, ALBIS fabricated a **new generation of photodiodes with integrated backside lenses which are used as "add-ons" in the hybrid integration platform**. AIFOTEC is responsible for **hybrid assembly** of the monolithic chips. HHI and FINISAR perform the **RF modelling to extend the electrical interconnection speed on chip and board level as well as within the Tx/Rx module packages**.

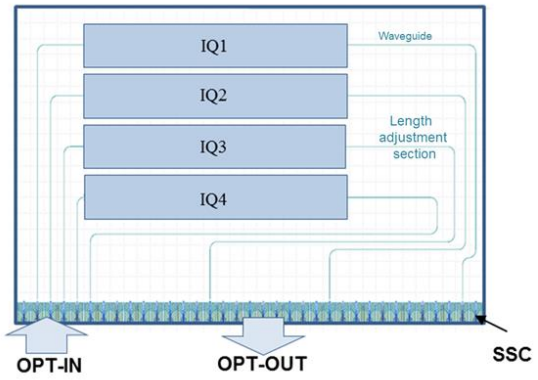


Figure 2: Schematic of the SSC-integrated and flip-chip ready quad-IQ MZ modulator PIC as basic active building block in the optical transmitter board.

The fabrication process of ASTRON photonic devices is completed with the **development of advanced planar passive optical waveguide structures** (iDFT/DFT AWG, 90^0 hybrids, optical power splitter/combiner, mirrors) on silica (glass) motherboard by partner OPTOSCRIBE.

RM3, AIT, OPTRONICS and TECHNION supported this technology development by **developing modelling and simulation tools** to effectively simulate the design and fabrication of the ASTRON devices. Moreover AIT in close cooperation with UCL and TECHNION developed all the **electronic circuits, necessary to drive and control the developed optical modules**. FINISAR brings to the group its industrial perspective and experience on such device fabrication, ensuring that the processes developed and materials chosen are **scalable to volume production and sensible from an environmental standpoint**.

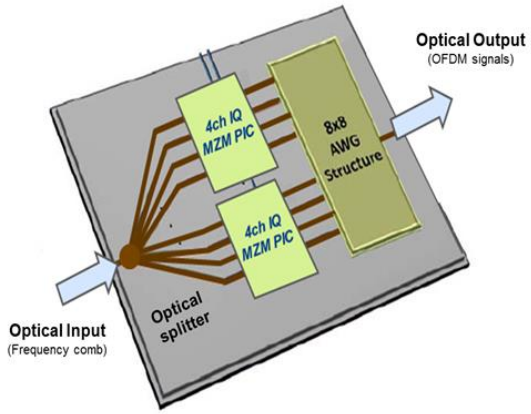


Figure 3: Schematic of the novel integrated multi-channel terabit capacity transmitter board

At each testing phase, ASTRON prototypes were delivered to the consortium corresponding beneficiaries for performing necessary characterization tests, after pigtailing and packaging done by OPTOSCRIBE, AIFOTEC and FINISAR. Performance characterization of the fabricated devices on a subsystem-level is carried out in each iteration by FINISAR, UCL, AIT, RM3 and TEI, which are top institutes in the field of optical fibre communications. Through this work, these beneficiaries provide experimental feedback to the design and fabrication stages and work in close collaboration with the respective beneficiaries. At the

final stage of the project, FINISAR, UCL, AIT, RM3, TEI and TECHNION will join resources in order to combine all the ASTRON devices and **assess their system-level performance in advanced test-beds** and transmission environments.

The system and component vendor point of view is continuously present throughout the duration of the project by TEI and FINISAR respectively so as to steer the activity technology exploitation of ASTRON and provide critical inputs on this. In collaboration with AIT, TEI, HHI and FINISAR carried out **techno-economic analyses and market driver studies** in order to build a solid base for the commercialization of the devices that will be exploited after the completion of the project. TEI and FINISAR also provide appropriate studies to define the required cost/performance relationship of the ASTRON devices necessary, guaranteeing that ASTRON devices will generate significant market interest and be competitive in the photonic components market. Once the ASTRON devices have achieved performance that warrants commercial evaluation, network performance of the devices will be evaluated from NICT using its high class test-beds and the Japanese national photonic network JGN-X.

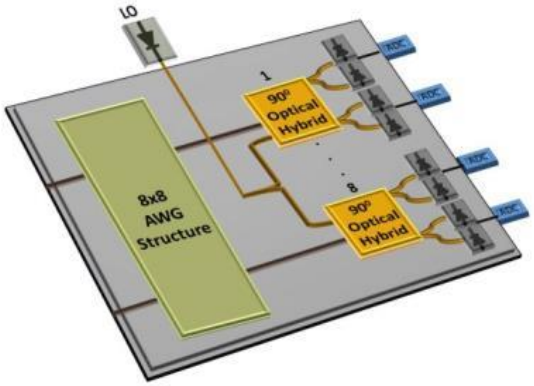


Figure 4: Schematic of the novel integrated multi-channel terabit capacity coherent receiver board

Achievements and Progress beyond the State of the Art

In the framework of the ASTRON project, two complementary configurations of Terabit OFDM transceivers were proposed, allowing energy-efficient and bit-rate flexible operation with rates from 10 Gbps to beyond 1 Tbps.

System Architecture and Requirements

The ASTRON concept combines monolithic and hybrid integration to develop, for the first time, complex super-channel OFDM/Nyquist-WDM transmitters and receivers relying on integrated arrayed waveguide gratings (AWG) for performing the inverse discrete Fourier transform/discrete Fourier transform (IDFT/DFT) in the optical domain. The two complementary configurations (OS-OFDM and AO-OFDM) are shown in Figure 5, the main difference being that the position of the splitter/combiner and the AWG are reciprocally inverted. A variant of the AO-OFDM scheme using single polarization and direct detection (DD) without chromatic dispersion compensation was also investigated for access/metro networks in compliance with existing (and coming soon) passive optical network (PON) standards.

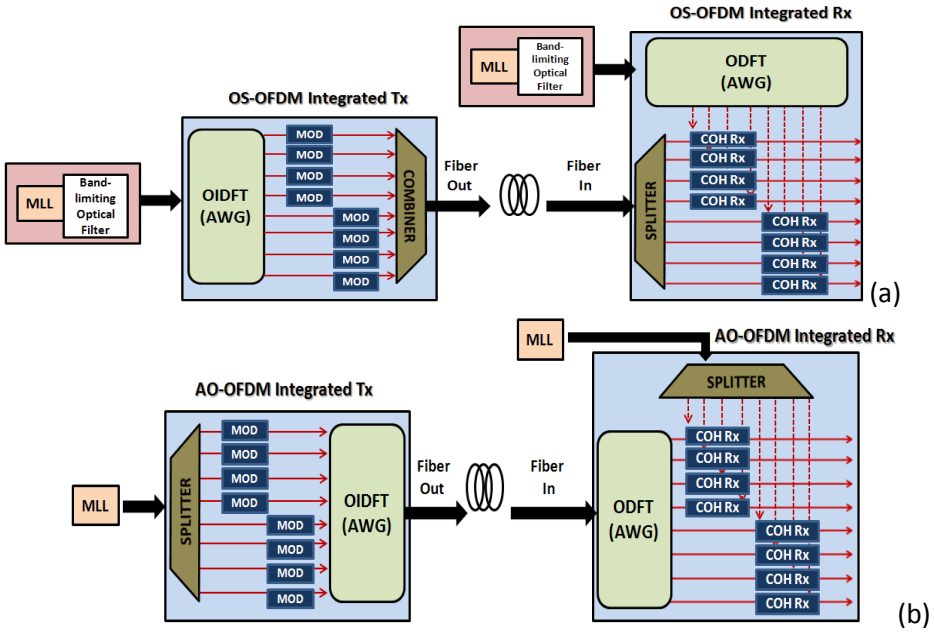


Figure 5: OS-OFDM (a) and AO-OFDM (b) transceiver architectures. MLL: Mode-locked laser.

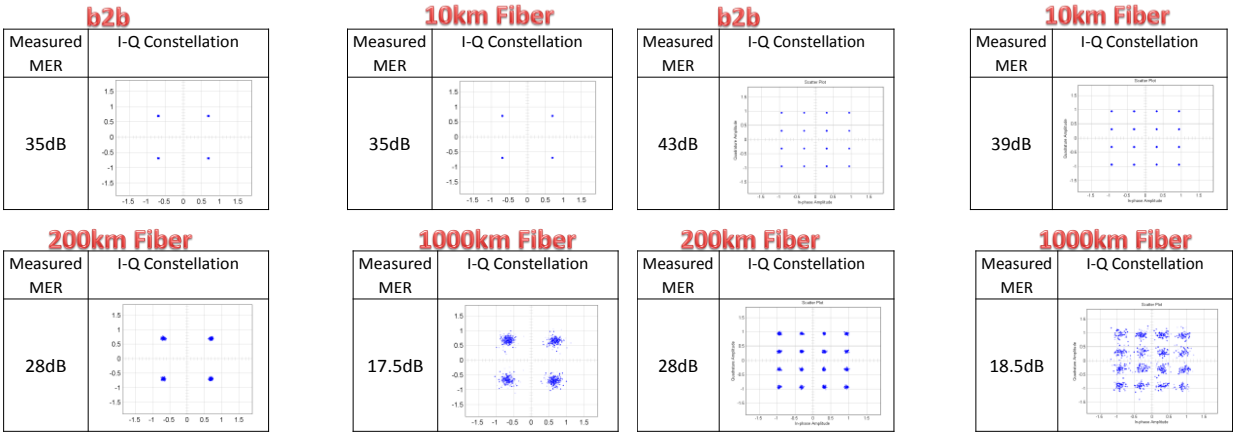
We assumed superchannels composed of eight subchannels confined within a total spectral width of 200 GHz. The transmitter and receiver specifications of the proposed solutions are listed in Table 1 and Table 2.

Table 1: Transmitter specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating wavelength range	λ	C-band	1528	1550	1570	nm
Optical bandwidth		3dB	25			GHz
Baud rate			28			Gbaud
Insertion loss	In Maximum transition regime				32	dB
Polarization dependent loss	|Loss(X)-Loss(Y)|			0.6		dB
RF drive voltage	Vπ				4	Vpp
DC extinction ratio for parent MZI			22			dB
DC extinction ratio for child MZI			20			dB
Optical delay between X and Y			-1		1	ps

Table 2: Receiver specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating wavelength range	λ	C-band	1528		1570	nm
Average optical input power	P_{sig}		-24		6	dBm
Baud rate	PM-QPSK		28			Gbaud
3dB cut-off Frequency	f_{3dB}			25		GHz
Average Photodiode responsivity	R_{avg}	CW single input			120	mA/W
Common mode rejection ratio	$CMRR_{SIG}$ $CMRR=20\ log(\Delta I_{PD}/\Sigma I_{PD})$	DC		-20		dBe
Imbalance	I_{Sig} I_{LO}	DC DC			2 2	dBo
Phase deviation	Δϕ		-5		+5	deg
Polarization extinction for Sig/LO	PER			20		dBo



(a) (b)

Figure 6: Received QPSK (a) and 16QAM (b) constellations for the OS-OFDM system performance in case of: back-to-back and at 10, 100, 200 and 1000 km.

A techno-economic analysis was also carried out for the ASTRON solutions, which were compared to other super-channel transceiver implementations. In Figure 7(a) we present the design of the OS-OFDM transceiver, and in Table 3 its estimated relative cost are shown. In Figure 7(b) & (c) we compare the cost of several superchannel transceivers and conclude that integration and packaging are determining factors in making the ASTRON solutions viable from a cost perspective.

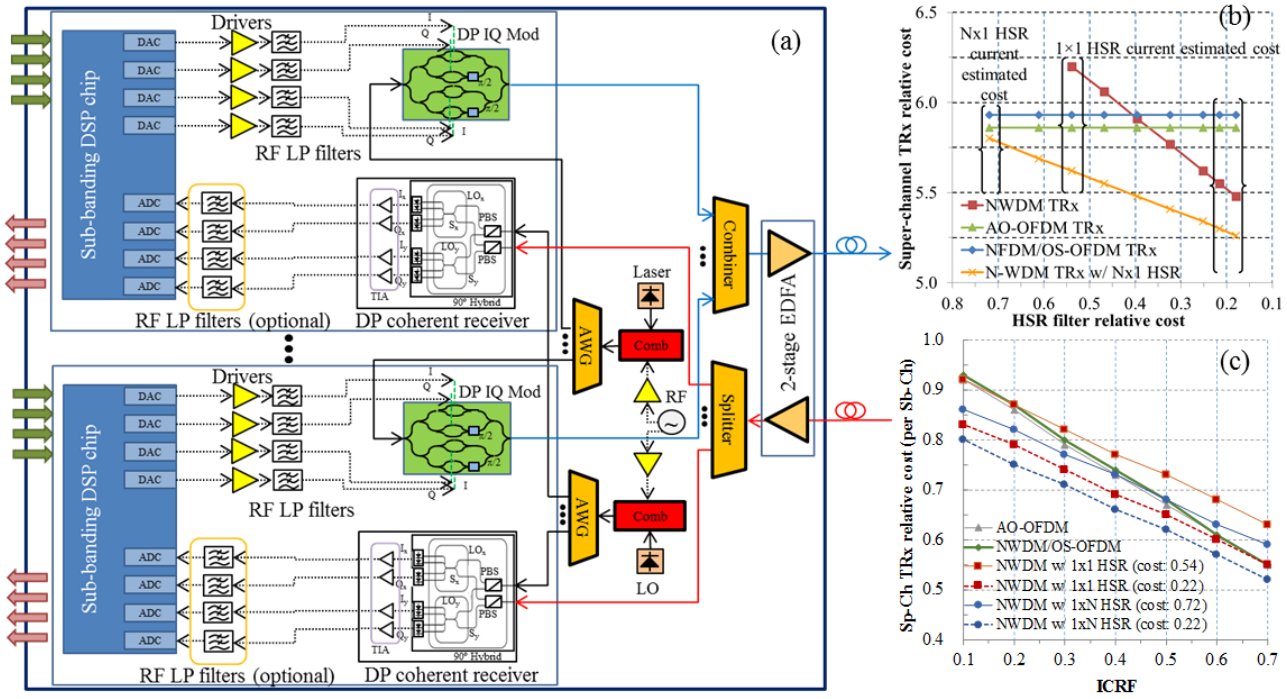


Figure 7: (a) Design of an ASTRON OS-OFDM transceiver. (b-c) Sensitivity analysis of the relative cost of a superchannel transceiver composed of 8 subchannels for NFDM/OS-OFDM, NWDM with optical filtering (with either two 1×1 HSR filters and an interleaver or one N×1 HSR filter) and conventional AO-OFDM on (a) the relative cost of the High Spectral Resolution (HSR) filter and (b) the integration cost reduction factor (ICRF) accounting for chip integration and packaging savings. The HSR filter cost is assumed to vary from a relative cost of 0.54 (current estimated cost of a 1×20 WSS) to ~0.2. For reference, we also indicated the current cost of a 1×9 WSS. Costs relative to the cost of a 100G transceiver.

Table 3: Relative cost and power consumption of the OS-OFDM super-channel transceiver implementation. (*) Relative to cost of 100G transceiver. (**) Relative to cost of 10G transceiver

Component	Relative unit cost (*)	Power (W) [max]	#	Relative cost (*)	Relative cost (**)	Total power (W)
DSP Chip	0.36	30.0	8	2.88	15.04	240.0
PM IQ Mod	0.22	0.0	8	1.04	5.41	0.0
Laser (Tx & Rx LO)	0.05	1.5	2	0.06	0.34	3.0
4-Port Modulator Driver	0.07	6.0	8	0.35	1.80	48.0
RF LP filter	0.00	0.0	64	0.14	0.72	0.0
DP Coherent Receiver	0.22	1.5	8	1.04	5.41	12.0
Variable gain dual-stage amplifier	0.18	12.0	1	0.11	0.56	12.0
Comb generator modulator	0.18	0.0	2	0.22	1.13	0.0
Comb generator mod. driver	0.07	2.0	2	0.09	0.45	4.0
1:N AWG	0.02	0.0	2	0.02	0.11	0.0
				5.93	30.98	319.0

The ASIC module represents 20%-50% of the total transceiver cost depending mainly on (a) the employed CMOS technology and (b) whether or not system vendors have in-house DSP chip development capability, but also, to a lesser extent, on (c) integration and packaging savings and (d) the number of integrated sub-channels. In ASTRON we have estimated the ASIC to account for ~49% of the total cost, and therefore a reduction in the DSP cost of, say, ~40% would result in an overall transceiver cost reduction of ~27%. It is then clear that reducing the CMOS process size is, together with monolithic integration, the single most

far-reaching mechanism to reduce the transceiver cost. Moreover, using smaller CMOS process sizes would also have a massive impact on the overall transceiver power consumption since the ASIC accounts for more than 70% of the power consumption of the transceiver. This can be further enhanced by reducing the complexity of the DSP algorithms. We report in this document that the ASTRON-project filter-bank-based OS-OFDM super-channel solution can provide around 44% total-ASIC-complexity reduction in comparison with a conventional transceiver, while ensuring a good transmission performance (note that the DSP complexity in the ASTRON-project transceiver is fundamentally due to the receiver part). Modelling studies suggest that moving from 40nm to 20nm to 16nm would reduce the power consumption by approximately 30-40% in each process step, which combined with the savings brought about by the filter-bank approach, could enable energy savings slightly in excess of 70% with 20nm and up to 75-85% with 16nm. This would make it possible for an integrated super-channel transceiver to reduce its power consumption to that of a 100G long-haul line card –including OIF MSA module based on the 40nm CMOS technology, OTU framer and client modules (~150W)–, thereby dividing by eight the environmental footprint of the ASTRON solutions in comparison with transmission scenarios relying on currently available 100G single-carrier transceivers. For enhanced performance, nonlinear equalization methods have been investigated in ASTRON and their computational complexity and power consumption have been assessed.

Optical Transmitter

Active and passive transmitter building blocks

The design, fabrication and characterization of **monolithic 4-channel (Quad) and 8-channel Mach-Zehnder (MZ) In-phase Quadrature (IQ) modulator PICs (IQ PICs) on InP** was finished (Figure 8). These IQ PICs are used **as active building blocks** for hybrid assembly with the passive optical planar glass motherboard in work package WP6 (Fig. 2,3). The board integrates all passive optical transmitter (Tx) functions of the hybrid 8-channel OFDM/N-WDM ASTRON transmitter planar lightwave circuit (PLC).

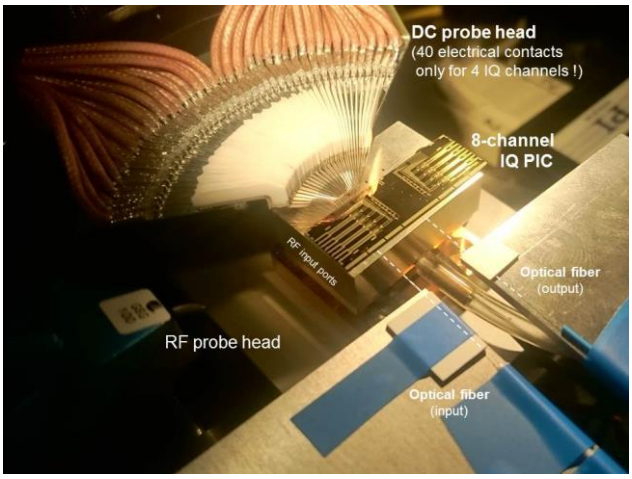


Figure 8: Photograph of two 4-channel (Quad) IQ InP PICs connected to a specifically designed and fabricated electrical 44-lines DC probe head while measuring the electrical performance characteristics on the test station. The electrical RF probe head is also shown as well as the optical input/output fibers attached to a single PIC interface.

The measured electrical dark currents in the modulator phase, travelling wave electrode (TWE) and monitor diode sections are too high in comparison with the typical data of discrete TWE MZ and IQ TWE MZ modulators fabricated at HHI. This behavior is not typical for modulator fabrication at HHI and therefore was not expected. The present high dark currents can reduce the device yield, because the IQ bias and operating points cannot be properly adjusted on the PICs. But this is currently proven.

Nevertheless, the current dark currents represent no fundamental PIC problem in general and the other device characteristics are already very promising.

The driving voltage Vπ of the integrated MZ modulators (child) within each IQ configuration (parent) is 2.3 ± 0.4 V. The overall optical insertion loss is 14.5 ± 1 dB at 1550nm wavelength (including long waveguide length adjustment sections for phase synchronization!). Small signal electro-optical response (S21) measurements reveal 3 dB bandwidths of 32 ± 5 GHz (Figure 9). The corresponding S11 characteristics are below -15 dB up to 45 GHz. A clear open OOK eye of an integrated MZ modulator at 40 Gb/s with an SNR above 12 dB and extinction ratio larger than 13 dB was observed (Figure 9). The small signal response characteristics are comparable with those of single standard IQ devices fabricated at HHI for commercial applications. It should be pointed out that these reference IQ devices do not integrate the additionally integrated specific electrical RF connection lines and termination resistors as shown in Figure 17. These specific electrical elements have been integrated in ASTRON TWE IQ MZ modulator arrays for the first time. This is already a very excellent result. Electro-optical 3 dB bandwidths of 42 ± 3 GHz have been achieved with an improved MZ modulator design on the same wafer.

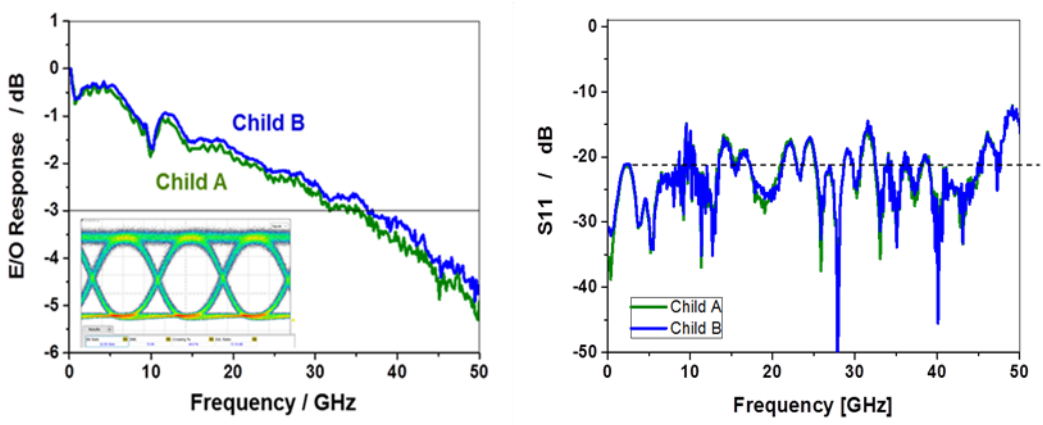


Figure 9: Electro-optical S21 and electrical S11 vs frequency of upper (child A) and lower (child B) MZ modulator in an IQ configuration, and a clear open MZ modulator eye diagram at 40 Gb/s.

The passive optical components required to implement the hybrid ASTRON transmitter are a 1x8 power splitter and an 8x8 AWG which were fabricated in a glass motherboard using 3-dimensional direct laser inscription.

The 1x8 splitter design is based on a 3-stage 1x2 Multi Mode Interference (MMI) coupler configuration. For fabricated splitters low excess losses per splitting stage of 0.8 dB and a good output power uniformity of 0.5 dB have been achieved.

The AWG was fabricated in glass according to the design schematic in Figure 10. The component is designed to deliver 8 channels, spaced at 0.2 nm within the 1.6 nm (200 GHz) Free Spectral Range (FSR). Specific data measured from a fabricated AWG are shown in Table 4.

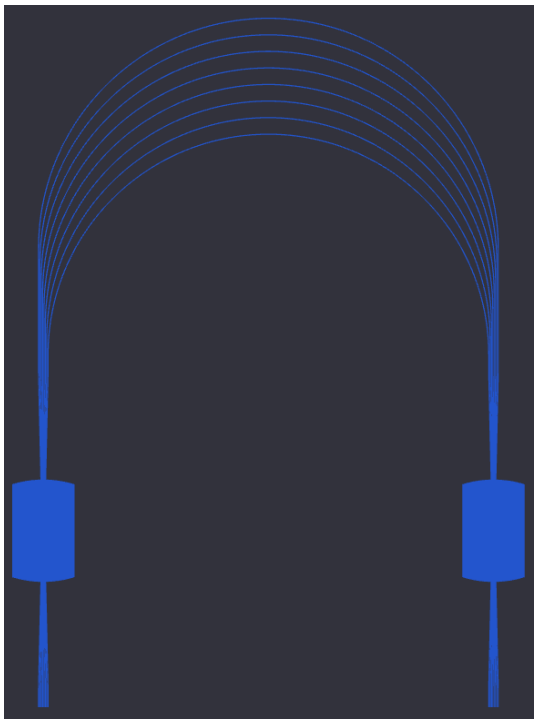


Figure 10: 8x8 AWG layout.

Table 4: Output channel peak data taken from device fabricated as per the layout shown Figure 10.

Diffraction Order	Channel	Peak Wavelength (nm)	Channel Spacing (nm)
m	1	1548.60	-
	2	1548.79	0.19
	3	1548.98	0.19
	4	1549.18	0.20
	5	1549.35	0.17
	6	1549.54	0.19
	7	1549.70	0.16
	8	1549.90	0.20
m+1	1	1550.16	0.26
		FSR =	**1.56**

As can be seen from Table 4, the fabricated device had 1.56 nm FSR and the maximum deviation from design of the wavelength peak was 0.06 nm. The insertion loss per channel was 18 ± 1 dB. Due to the use of the mode-locked laser in the ASTRON transceiver, the crosstalk (XT) in the AWG is defined as the minimum difference between the power at channel peak wavelength and the power in the two adjacent channels measured at the same wavelength. The XT values measured in the fabricated device were between -3 dB and -5 dB. However, the AWG devices available at project end meet the target specifications of 1550 nm center wavelength, 200 GHz free spectral range (FSR) and 25 GHz channel spacing precisely within given error margins. The AWG loss and crosstalk have to be further improved

mainly in order to enable good Tx operation. Possible improvements to component fabrication have been identified.

Hybrid Integration of the Transmitter (PIC-on-Glass)

In the **PIC-on Glass (POG)** hybrid integration approach, the active InP IQ Mach-Zehnder modulator array chips are directly assembled onto a glass board as common integration platform by using flip-chip eutectic bonding and precise pick-and-place techniques. The optical glass board integrates all required passive optical Tx functions (splitter, AWG, retiming) as well as all required electrical DC and RF tracks and connections. In particular, the novel Selective Laser Induced Chemical Etching (SLICE) process, shown in Figure 12, proposed by Optoscribe for optical Tx glass board fabrication offers advantages with respect to other commonly used fabrication techniques. The key benefit of this process is the simultaneous fabrication of the passive waveguide circuits and the required etched recess areas and stand-off features. Thereby recess and stand-off levels are inherently aligned to the waveguides. The stand-offs are also required to support the large-area modulator PICS during flip-chip bonding.

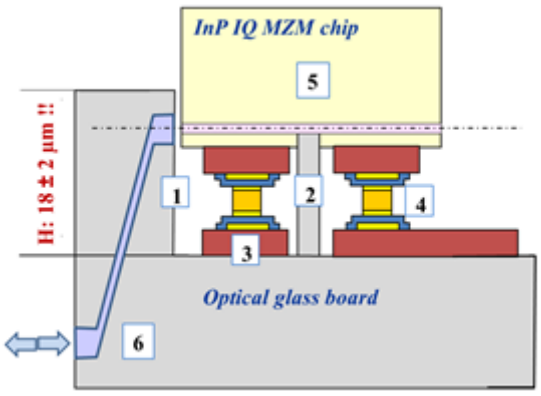


Figure 11: Schematic cross-section depicting an InP-based IQ Mach-Zehnder modulator chip assembled onto the optical glass board as common integration platform. (1: Deep recess with vertical side walls at optical chip-board facet (H= 15…22 µm !!), 2: Stand-off features for vertical chip alignment, 3: Electrical DC/RF tracks/pads on the deeply etched glass board level, 4: AuSn solder bumps for flip-chip bonding, 5: InP-based IQ MZM chip, 6: Vertical transition of optical board waveguide from the board waveguide level (-50µm) up to the required level in the chip region) (Source: HHI)

Figure 12 shows the successful surface profiling of a glass test wafer to create the stand-off features. Wafer-scale application of the SLICE process has been demonstrated to produce the required surface profile with base layer depth of 30 um. Reducing the base layer depth to less than 21 µm was required for the subsequent lithographic processing of the RF transmission lines. This reduction prevented proper formation of the recess profile during the wet etch processing step despite exhaustive engineering efforts in refining the wafer mounting and characterisation accuracies such that flatness could be confirmed to within 0.5 µm across the full surface of wafers up to 4-inch in diameter.

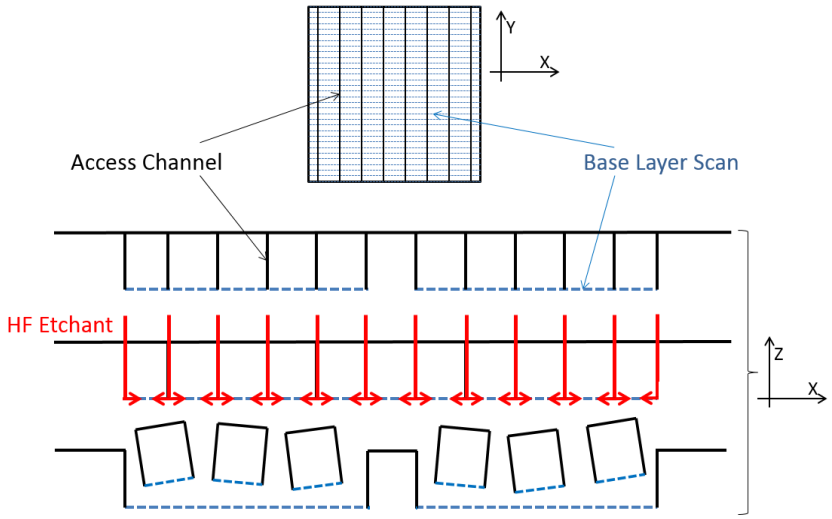


Figure 12: ***Wafer-Scale SLICE Processing. Base layer scans are patterned first. Multiple access layers are patterned in vertical stacks to enable HF etchant to proceed down to the base layer depth and then laterally along the base layer scans. The strips of glass material are thereby removed to leave only the standoffs which will support the PIC.***

Figure 13 shows the successful surface profiling of a glass test wafer to create the stand-off features.

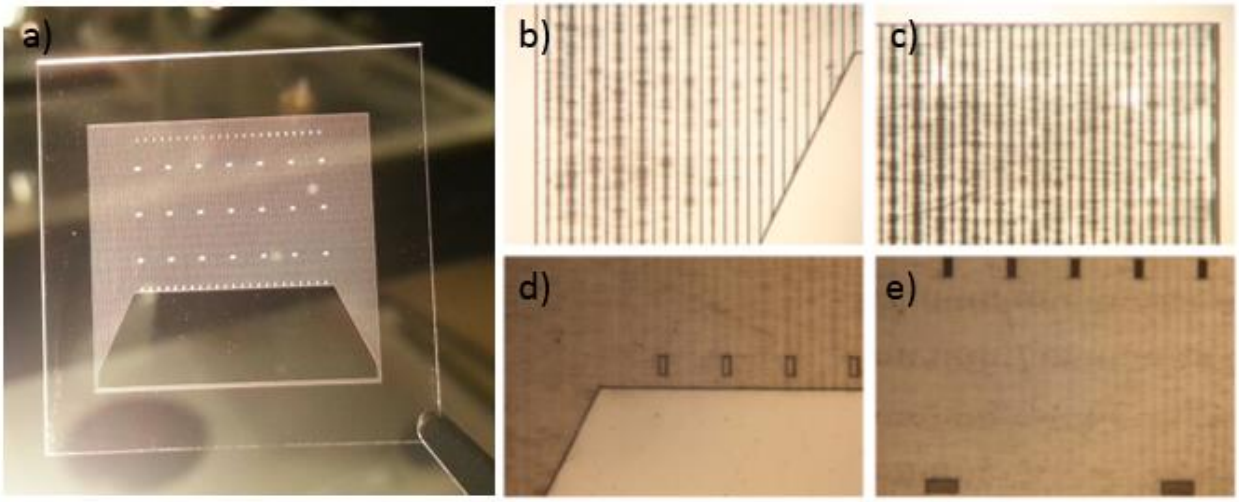


Figure 13: **a)** ***Photograph of SLICE trial layout patterned on 25 x 25 mm wafer. The mesa (trapezoidal area) is unpatterned. b) & c) The vertically oriented access channels can be seen along with the lateral progress of the etchant solution along the 30 µm deep base layer.***
d) & e) Fully ethched test die. Electrical layer is visible along with the stand-off tops and unmodified mesa (trapezoidal section).

PIC-to-Glass (PTG) concept

The PIC-to-Glass (PTG) concept was introduced in order to avoid the surface profiling of the glass board which is a necessary first step in the POG hybrid integration concept described above. The first step of the PTG scheme the InP IQ PIC is mounted on a suitable carrier (Si) as shown in the first step of Figure 14. The InP IQ PICs contain suitable alignment marks and features which can be detected by the laser inscription system in order to determine the specific lateral and vertical coordinates of the waveguides in the PIC. Due to this measurement the unavoidable PIC bowing which is introduced after the first assembly is calibrated in order to generate a bespoke glass board. Thereby, the optical waveguide input ports on each glass board can be precisely tailored to the specific coordinates of the output ports of the PIC waveguides on each particular assembly. The glass board is then actively aligned and bonded to the associated PIC on carrier as shown in the second step of Figure 14. Finally, the sub-assembly is mounted onto a common

carrier which can support the DC and RF PCBs for electrical connection to the modulators and can be mounted onto the TEC in the module package as depicted in Figure 15.

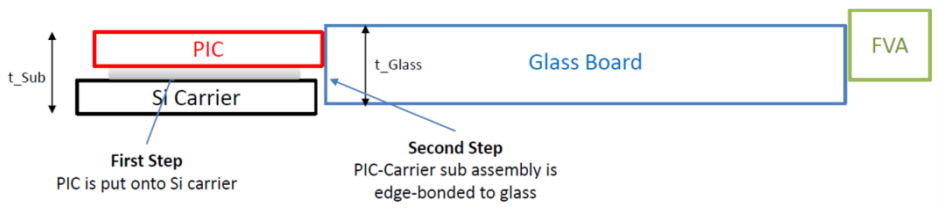


Figure 14: Schematic cross-section view of PIC-to-Glass hybrid coupling scheme.

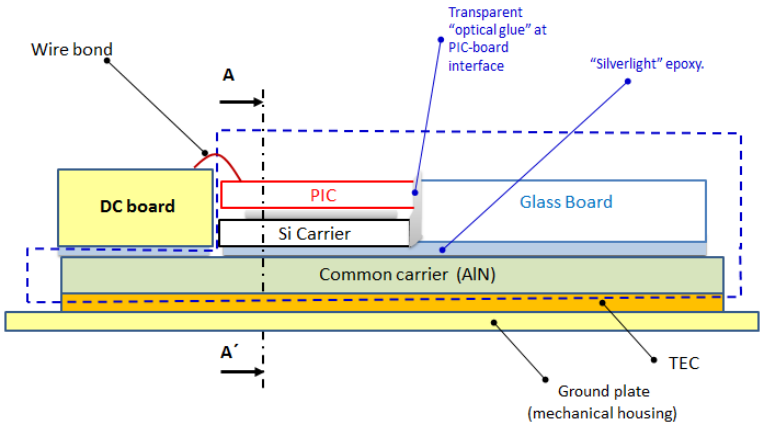


Figure 15: Schematic cross-section view of the final assembly: Modulator PIC mounted on Si carrier, edge coupled to the glass board and finally mounted on a common carrier which supports DC and RF (not shown) planar connection boards (PCBs).

The assembly shown in Figure 16 was the proof-of-concept demonstration of the PTG hybrid scheme. During the assembly process it became evident that a geometry mismatch existed between the waveguide positions in the glass interposer and PIC and this resulted in high insertion losses. The accuracy of the waveguide positioning during laser inscription is certainly sub-micron and therefore the geometric error was a result of the measurement error in the calibration step which determined the PIC assembly bowing. Refinement of the PIC calibration method should lead to sub-micron positional accuracies significant reduction in the optical coupling loss.

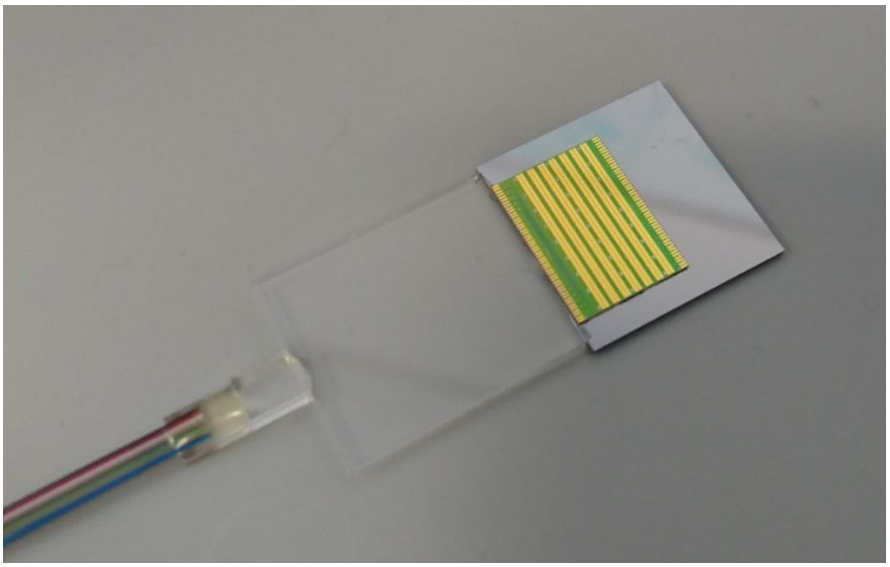


Figure 16: The first PTG assembly fully attached with an optical fiber array.

Monolithic Integration of the Transmitter

As an alternative transmitter fabrication approach to the hybrid concept, fully integrated 8-channel OFDM/Nyquist-WDM Tx PICs on InP have been designed, fabricated and characterized in WP3 (Figure 17) [3]. In particular, these Tx PIC architectures integrate:

- An 1x8 optical splitter at the PIC input port
- Eight nested travelling wave electrode (TWE) Mach-Zehnder IQ modulators as in the fabricated 4(8)-channel IQ PICs described before; i.e. also consisting of electrical RF 50 Ω termination resistors and specific CPW/CPS transitions
- An 8-port AWG to perform optical IDFT and signal multiplexing/de-multiplexing
- Several phase sections and GaInAs photodiodes for setting of IQ operating points and monitoring purposes
- Optical waveguide length adjustment sections for signal (phase) synchronization and uniform power levels in each Tx channel

The CAD mask layout and a photograph of a fully integrated 8-channel AO-OFDM InP transmitter PIC is depicted in Figure 17 (on the right).

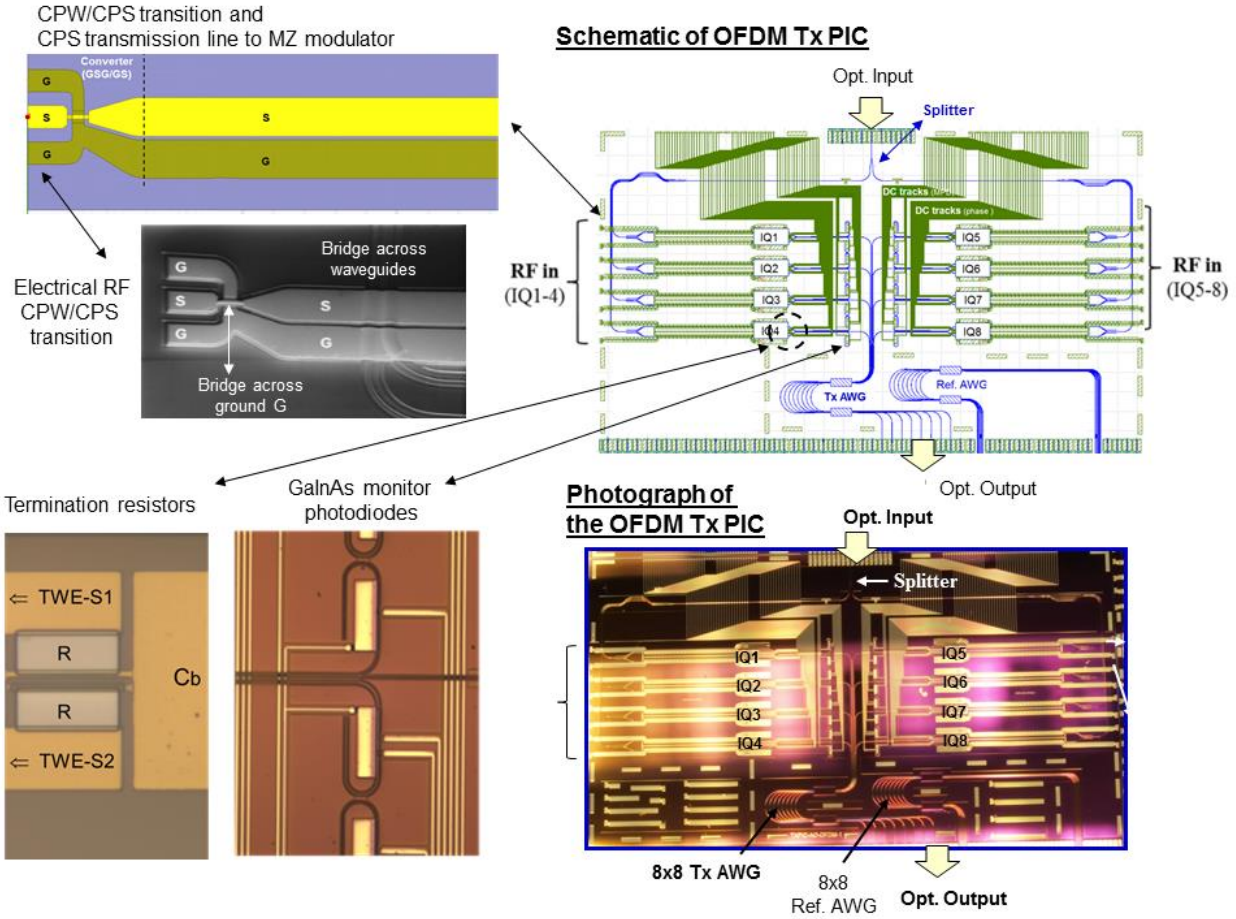


Figure 17: Schematic and photograph of a fabricated AO-OFDM Tx PIC integrating a 1x8 optical splitter, eight TWE MZ IQ modulator channels, and an 8-port AWG as main building blocks (right). Integrated monitor photodiodes as well as electrical 50Ω RF termination resistors and specific CPW/CPS transmission lines/transitions are shown on the left.

The additionally integrated specific electrical elements are shown on the left in Figure 17. The achieved optical performance data of the critical 8-port AWG are summarized in Table 5. The AWG target specifications are not completely met after this very first fabrication run. But further design and

technology optimization will improve the spectral transfer characteristics. The MZ modulator performance is similar to those of the 4(8)-channel IQ PICs presented above.

Table 5: Compilation of experimentally determined AWG performance data in comparison with theoretical data and ASTRON target specifications

	ASTRON specs	Theory	Exp. (best)	Exp. (average)
FSR [GHz]	200	200	175.8 ± 1.7	176 ± 5
Channel spacing / GHz	25	25	22.3 ± 1.3	22.5 ± 2.5
Excess loss / dB	≤ 12	≈ 11	14 ± 1	14.3 ± 2.4
Power uniformity / dB	≤ 5	1.3	1.8	1.5 ± 0.3
ICI / dB	≥ 12	25	8.3 … 10.5	7.5 dB ± 3 dB

Particular attention needs to be paid to the overall optical PIC insertion loss in each IQ channel. First measurements revealed an insertion loss of ≈ 35 dB. But further loss reduction is achievable by subsequent optimization of the passive optical Tx PIC building blocks (mainly waveguides and AWG). The estimated IL data of the hybrid ASTRON Tx have been found to be almost within the same range, provided that a low coupling loss is achievable at the Tx board and IQ MZM PIC interfaces. But even for a similar transmitter set up, which is established by connecting different discrete and commercially available modules, an almost similar insertion loss has been estimated. However, the considered hybrid and module based transmitter fabrication approaches have almost the same optical insertion losses per IQ channel as the fabricated Tx PIC on InP, but without the benefit of a very compact architecture fabricated on a very small scale.

In summary and to the best of our knowledge, the AO-OFDM but also the OS-OFDM transmitter configuration has been monolithically integrated in InP for the first time worldwide in the ASTRON project.

Transmitter module

A module package layout was made available, as well as the required electrical 8-channel RF connection boards that were designed, fabricated and tested. However, it was not possible at the end to package either a hybrid 8-channel OFDM Tx PLC or a monolithic Tx PIC into a fiber-pigtailed transmitter module. The main reasons for not achieving this, despite the huge efforts in that direction by the ASTRON components fabrication partners, are summarized and explained as follows:

- The complexity of the hybrid - as well as of the monolithic - core piece within the proposed 8-channel OFDM transmitter module was identified as too high with respect to the available experimental know-how at project start in terms of design, fabrication technology (glass board technology), fabrication yield (on glass and InP), and characterization effort (Tx PIC).
- When looking back, the unavoidable switch to a completely different board technology on glass wafers at project start was already a very challenging task. On the other hand, the introduction of the novel SLICE process suggested by the new partner Optoscribe was very promising; not only for ASTRON but also for other future hybrid large scale device developments. But the development of the SLICE process as well as the integrated passive optical Tx subelements (splitter, AWG) became more difficult than expected. Nevertheless, a lot of experiences have been gained and represent a good basis for further improvement. But further improvement was not possible within the remaining ASTRON project time because of required effort and time. Thus the consortium decided to go ahead with two alternatives in the final project phase to provide at least a hybrid transmitter component: The hybrid PTG approach and the monolithic Tx PIC on InP.
- The demonstration of the PTG approach has been presented finally. But further improvement as well as the fabrication of a passive optical Tx glass motherboard was not possible.

- The fabrication and characterization of both proposed Tx configurations as monolithic Tx InP PICs have been successfully achieved. Because of fabrication yield, required characterization effort and available time it was not possible to package either an AO-OFDM Tx PIC nor an OS-OFDM Tx PIC into a fiber-pigtailed module at project end.

In any case, the challenges in delivering a fully packaged prototype led the consortium to develop innovative alternative fabrication approaches and realizations which enabled the involved partners to gain considerable knowhow that would be very useful in their product development activities and future endeavors to realize integrated small-form-factor transceivers.

Optical Coherent Receiver

Balanced InP based 25 Gb/s photodiode arrays with a monolithically integrated backside lens and an optimized RF layout were developed as the basic active receiver building block. First samples of the photodiodes have been manufactured and tested. The performance characterization shows that the developed photodiodes are well suited for the ASTRON project application. Figure 18 shows photographic images of the topside and backside of the manufactured balanced photodiode array.

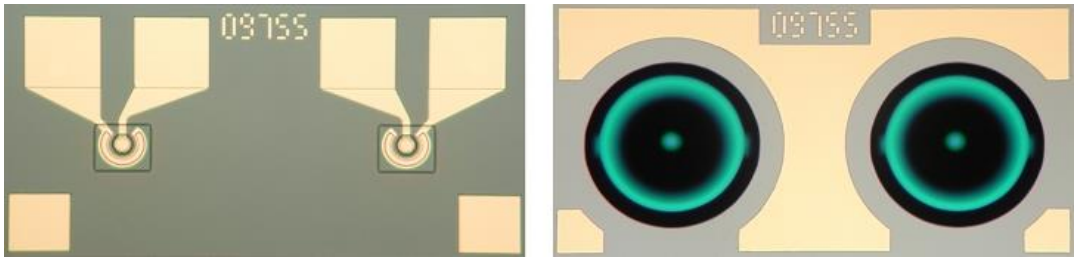


Figure 18: Photographs of the balanced PD array. Left: PD topside. Right: PD backside with integrated lenses.

Measurements in the time domain were performed to determine the eye diagram response of the fabricated photodiodes. The bit rate of the input signal was 28 Gb/s. All measurements were done at a wavelength of λ=1550 nm, the received optical power was P_{opt}= 0 dBm, resulting in an average photocurrent of about I_{PH}= 0.8 mA at different applied bias voltages ranging from V_R= -2 V to V_R= -5 V. The obtained eye diagrams can be seen in Figure 19. At this high bit rate the eyes are widely opened (Figure 18).

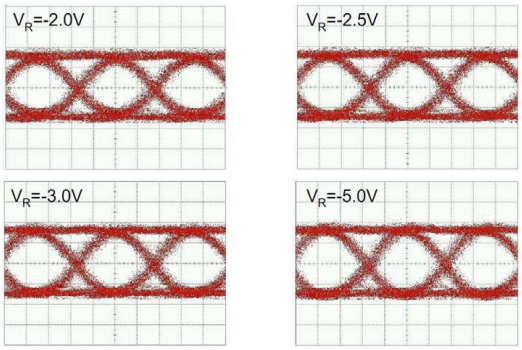


Figure 19: Detected eye diagrams at a bit rate of 28 Gb/s and different applied bias voltages. Optical input power was 0 dBm. Horizontal resolution is 10ps/div.

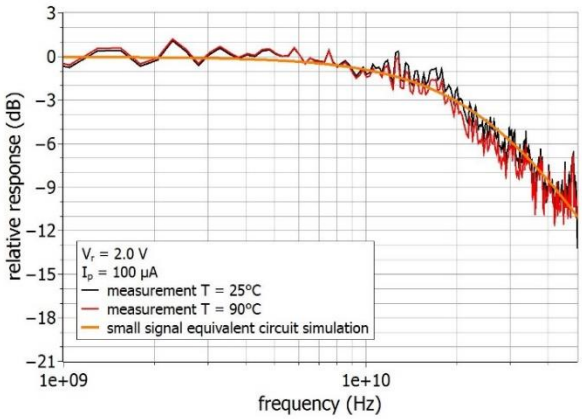


Figure 20: S12 - Frequency response measurements.

The 3dB-bandwidth of the photodiode is largely sufficient for 25 Gb/s operation even at a bias voltage of only V_R=-2 V. The simulation of the S12 frequency response using the calibrated small signal equivalent circuit shows good agreement with the measurement (Figure 19).

Hybrid Integration of the Receiver

PIC-on-Glass (POG) Hybrid Assembly of the Rx Platform

The assembly (eutectic bonding) of the photodiodes on the Rx glass boards is known as hybrid PD-on-Glass assembly approach. The mirrors couple the light out of the plane of the board and therefore hybrid integration of the single as well as dual channel 25Gb/s InP photodiodes onto the glass board is performed with the backside lens facing down at Aifotec. Figure 21 shows the schematic view of the assembly.

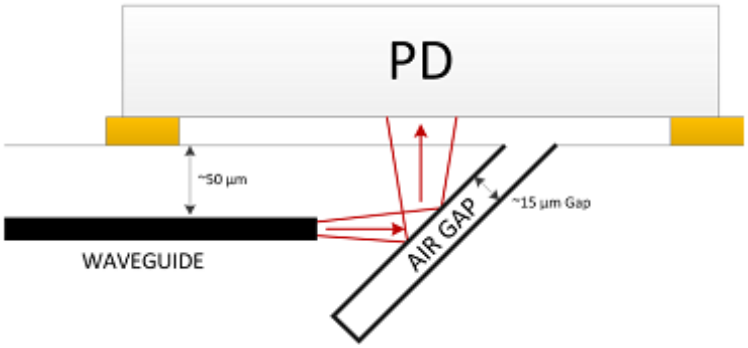


Figure 21: Schematic setup of the glass substrate with the 45° mirror and the photodiode.

Rx single and dual channel test glass board: The passive waveguide components and 45° inclined mirror structures are fabricated in the glass substrate by direct laser inscription. OPTOSCRIBE fabricated the silica glass test board. ALBIS and HHI deposited the different metallization layers for hybrid integration of the photodiodes. The necessary assembly features for hybrid integration of the photodiode onto the glass substrate include alignment marks, base metallization and AuSn solder-bump metallization (Figure 22). Dimension and size of the metallized pads are matched to the shape of the contact pads on the photodiode chip. The final hybrid assembly was then performed at AIFOTEC by laser-based spot-size soldering.

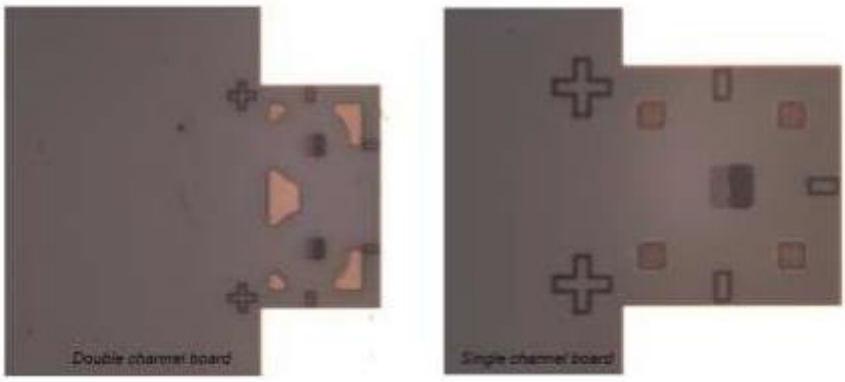


Figure 22: Microscope image of a double and a single channel test board

Final assembly of PDs on Rx test boards: 40 single-channel and 40 dual-channel PDs were bonded onto receiver test boards (fabricated on 4” glass substrate) at eutectic conditions of 305°C and 30g contact force. Figure 23 shows the PDs bonded according to these parameters.

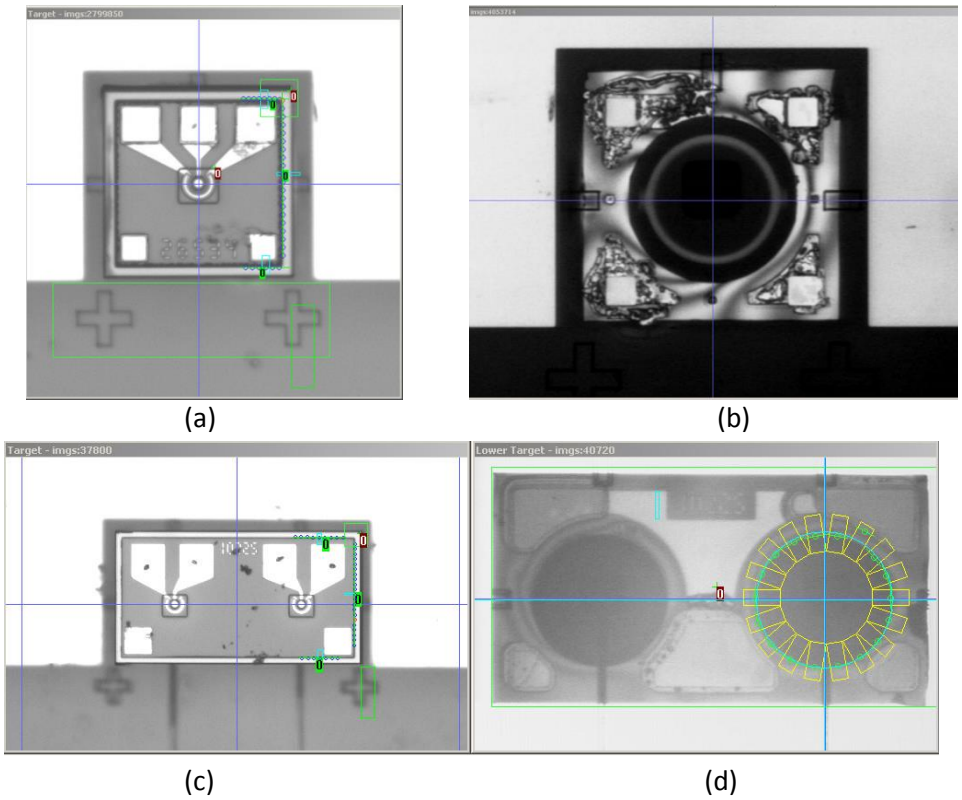


Figure 23: Top and Bottom views of bonded PDs on Single (a, b) and Dual channel (c, d) Rx test boards

As evident from Figure 23, good wetting was observed in all the assemblies and the shear strength obtained for the sample batch of 5 was within the acceptable range of >30g. The non-sheared PD-Rx board assemblies were shipped to Albis for first testing. It could be observed that the test boards are working properly but with very high coupling losses. Those findings were taken into account for the fabrication of the final Rx board.

Final Rx silica motherboard

The final ASTRON receiver motherboard layout (shown in Figure 24 incorporates an 8x8 AWG along with eight optical coherent receiver front-end circuits (consisting of the combined 90° optical hybrid and the 45° mirror structure) and a 1x8 power splitter.

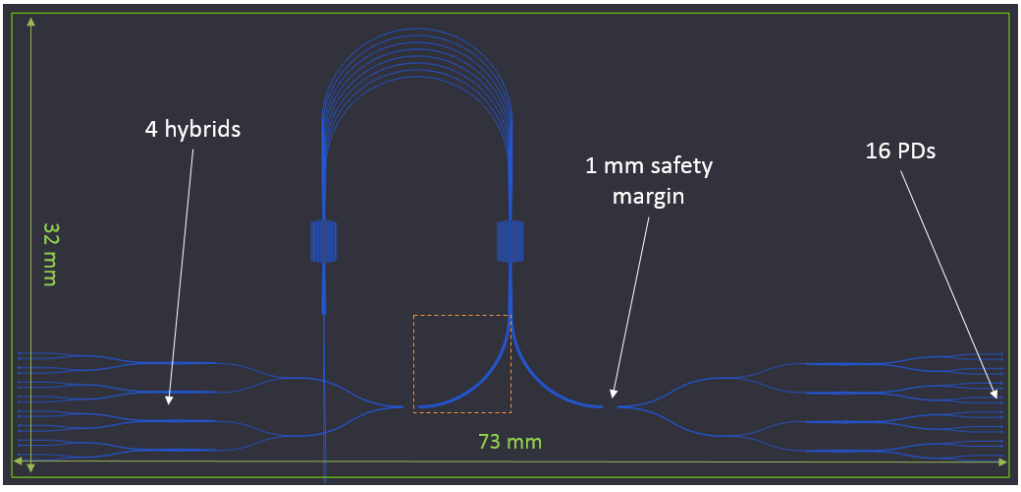


Figure 24: Final 8-channel receiver board layout.

The coherent receiver channels are separated into two banks of 4 channels. Each channel comprises of two balanced photodiode arrays with a total of four photodiode signal outputs as shown in Figure 25:

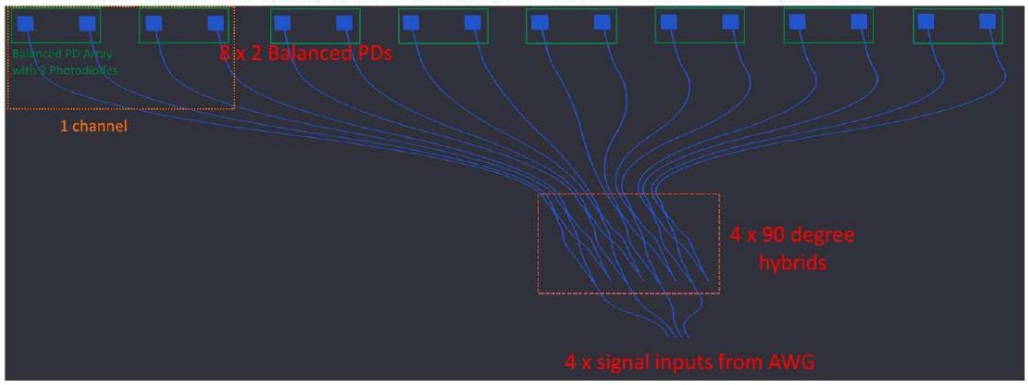


Figure 25: 4-channel building block for the final receiver motherboard.

The area of the photodiodes on the final Rx boards are bound to be without any geometrical changes with respect to the Rx test boards. Position of the alignment marks and pitch dimensions are the same as in the dual channel test boards used for hybrid assembly tests.

Fabrication of the final coherent receiver motherboard and subsequent hybrid integration of the high-speed balanced photodiode arrays is currently on-going and is expected to be finished soon.

RF transmission lines

In order to perform DC as well as RF measurements each single photodiode has to be connected to an electrical RF transmission line. The transmission lines will be integrated on a DC/RF PCB fan-out with suitable RF connectors. The PCB fan-out will be connected to the photodiodes with wire-bonds. The RF connector dimensions require that the DC/RF fan-out is made in two semi-circular parts and integrated separately on either side of the Rx board as depicted in Figure 26:

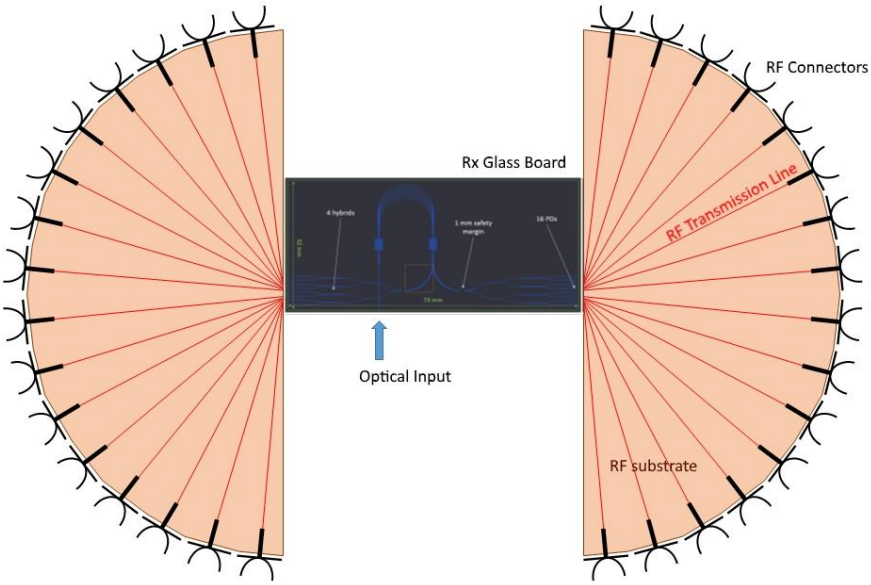


Figure 26: Schematic of the final Rx silica motherboard with RF PCB fan-out.

Software defined Signal Processing, Modulation and Control

The rationale behind the developed filter-bank based OS-OFDM transceiver is to break the digital processing into multiple parallel virtual sub-channels, occupying disjoint spectral sub-bands. Figure 27 shows the overall design of the receiver DSP which was implemented, while Figure 28 shows a top level view of the DSP algorithmic chain implemented within the OS-OFDM receiver [4].

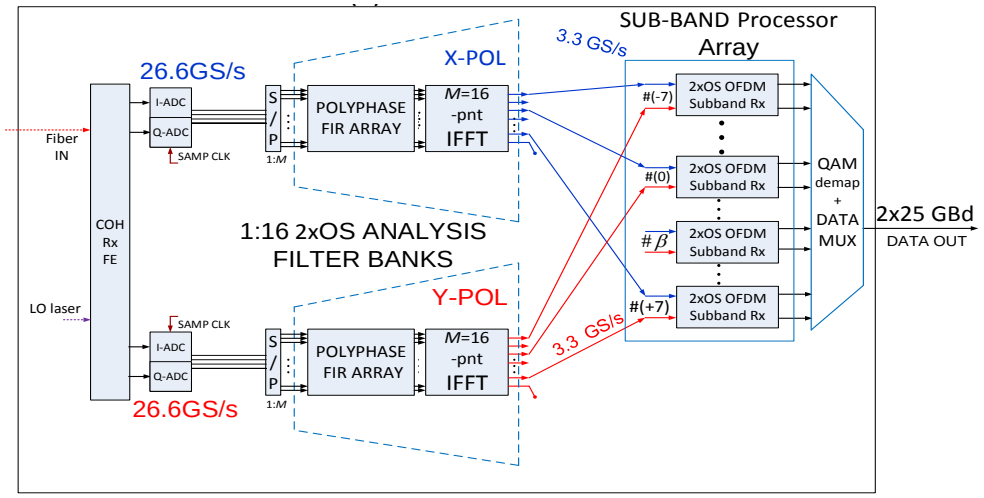


Figure 27. Schematic of the overall OS-OFDM receiver design.

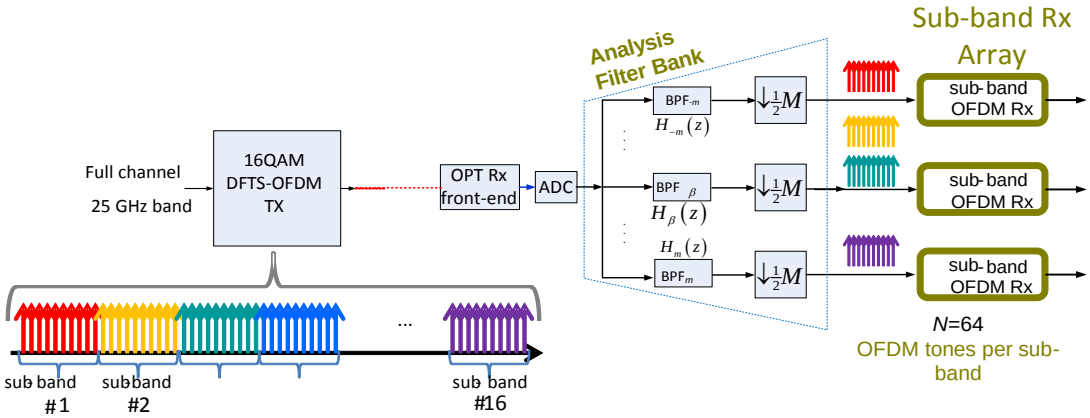


Figure 28. The basic diagram of the filter-bank based OS-OFDM DSP.

The main advantage of this transceiver is that the greater the number of sub-channels the more the delay spread due to chromatic dispersion (CD) is reduced, hence lowering the DSP complexity. It is shown that the ASTRON-project filter-bank based OS-OFDM superchannel solution provides more than 40% reduction.

However, this DSP solution only compensates for linear impairments. To enhance the DSP's capability to mitigate fibre impairments, we investigated in terms of performance the following nonlinear equalization techniques when applied in a single- and multi-channel equalization scheme:

- digital back-propagation based on split-step Fourier method (DBP-SSF)
- inverse Volterra series transfer function nonlinear equalizer (IVSFT-NLE)

The performance of multi-channel equalization schemes, namely 3rd-order inverse Volterra series transfer function nonlinear equalizer (IVSTF-NLE) and digital backpropagation based on split-step Fourier (DBP-SSF), over a 400 Gb/s DP-16QAM superchannel, formed by 9 quasi-Nyquist multiplexed channels, were compared. For a low number of channels being compensated, the IVSTF-NLE provides quite low Q^2-factor

improvement compared to the linear compensation, while the single-step-per-span DBP-SSF (DBP-SSF$_1$) seems to be the method of choice. However, in the equalization of multiple channels, the DBP-SSF method performs well only with a high number of steps (at least 40), introducing prohibitively high computational effort. On the contrary, the IVSTF-NLE performs similarly to the heavily iterative DBP-SSF$_{40}$ with only one SpS. Therefore, the IVSTF-NLE could be a promising candidate for the next generation high capacity long-haul terrestrial systems, offering relatively low implementation complexity, and consequently, lower power consumption.

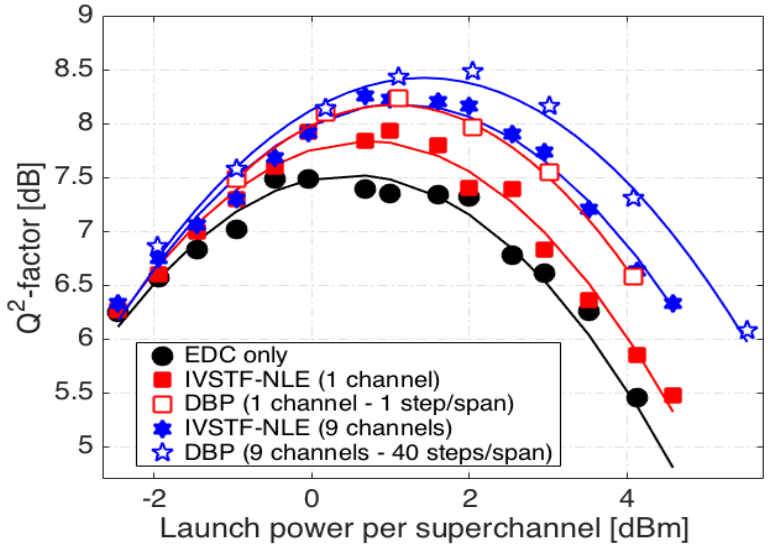


Figure 29. Q^2-factor as a function of the launch power when applying IVSTF-NLE, DBP-SSF$_1$ and DBP-SSF$_{40}$ to the single channel and 9 channels of the central superchannel after 20×80 km transmission distance.

Figure 29 shows that the performance of the all-band equalization scheme provides a ~1.88 dB Q^2-factor improvement while the band-by-band equalization scheme provides an ~1 dB, compared to linear case only. Thus, the implementation of IVSTF-NLE in an all-band equalization scheme exhibits superior performance compared to the band-by-band equalization scheme.

Additionally, we implemented DSP algorithms aiming at real-time demonstration of OS-OFDM using FPGAs. Optimization was carried out for the spectral structure of the OS-OFDM signals, the data structure, the filter bank module, the carrier frequency offset (CFO) mitigation, the receiver synchronization, and the equalization algorithms for multi-band polyphase filter banks for low-complexity reduced guard interval OFDM. Finally, these DSP algorithms were tested via offline processing. As a result, we obtained 16QAM constellations, after 80 km transmission reach, as depicted in Figure 30.

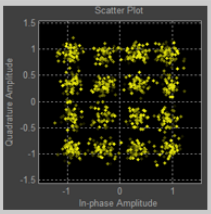
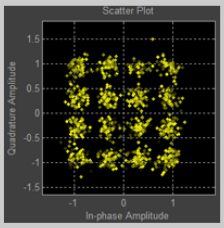
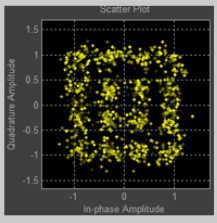
OSNR	24dB	24dB	24dB
LPF BW	8MHz	50MHz	150MHz
MER	16.5dB	15.7dB	14.5dB
Constellation			

Figure 30. Received signal constellations with different LPF BWs for CFO compensation. Acronyms: Low Pass Filter Bandwidths (LPF BWs), Modulation Error Ratio (MER).

FPGA-based Super-channel Transmitter

Detailed architectures of the implementation of the OS-OFDM transmitter and the receiver signal processors were delivered. We came up with the design, implementation and testing of the FPGA Digital-to-Analog Converter (DAC) subsystems and the analogue electronics that were used leading to the integration of the sub-system within the ASTRON transmitter. This involved the use of the FPGAs to drive the eight integrated InP IQ modulators at a symbol rate of 28 Gbaud. One possible scheme with the ASTRON transmitter photonic hardware is shown in Figure 31 that refers to the OS-OFDM configuration.

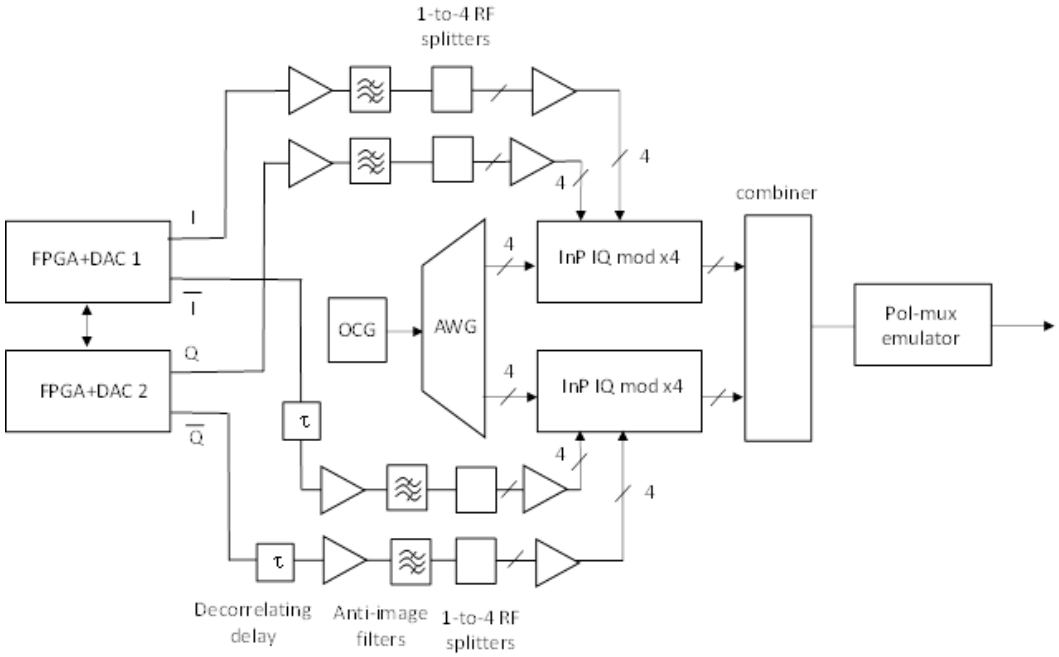


Figure 31. Proposed setup for ASTRON OS-OFDM architecture transmitter testing.

The DSP algorithms were implemented in a FPGA for overall demonstration of the system, and were shown to operate successfully in real time. The hardware implementation scheme of this algorithm is presented in Figure 31.

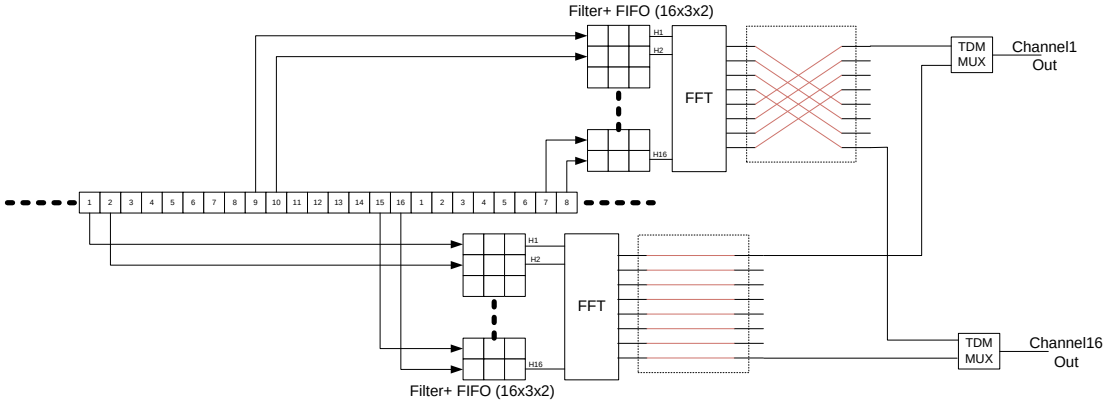


Figure 32. Hardware implementation of the filter-bank.

The rate of the filter bank is reduced by a factor of 16. While this rate is within the reach for current ASIC chips, it was necessary to reduce the hardware rate further for the FPGA implementation. Hence, we performed further slowdown by a factor of 4 to allow operation with clock rates of about 400MHz.

The ASTRON filter-bank receiver was built up using three FPGA located on three boards (Figure 32 for the high-level architecture and Figure 33 for the actual hardware).

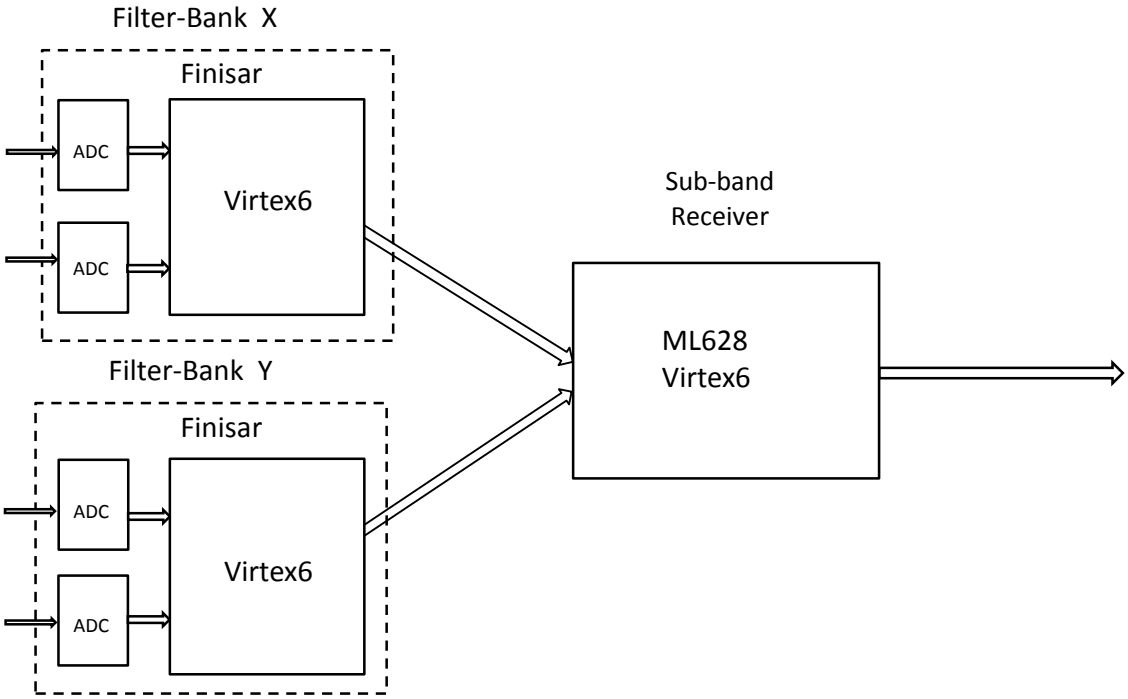


Figure 33. High level architecture of the ASTRON receiver.

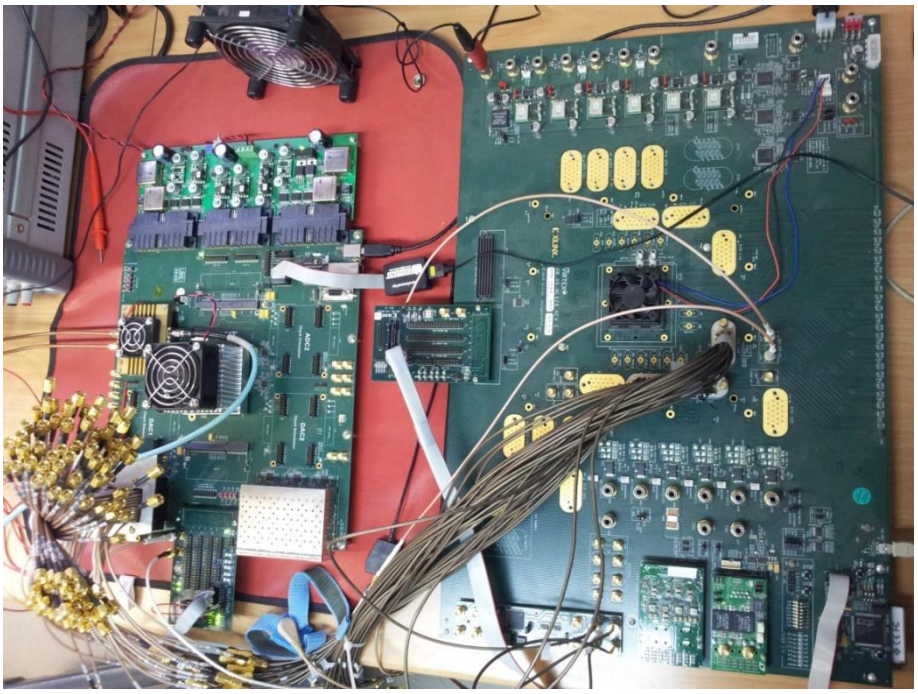


Figure 34. The integration of the filter banks with the sub-band receivers with those two boards.

All receiver functions are real-time implemented resorting to just 3 FPGA chips. FPGA X/Y interfaces to the ADC chips, performs calibration of internal ADC parameters and IQ gain/phase imbalance correction, at system bring-up. Following IQ- imbalance correction, the data is de-multiplexed into sub-bands. Sub-banding is performed on sets of 16 input samples; due to 2x oversampling, a factor-of-8 rate slow-down is attained. To evaluate system performance we measured EVM/EsN0 vs OSNR (Figure 35 left). A

dominant impairment was identified as quantization noise. The estimated ADC ENOB for both DAC and ADC was ~4bits. In actual measurements, the effective ADC noise was higher due to lack of adaptive pre-ADC AGC stage. The maximally attainable estimated SNR was ~18dB. Beyond back-to-back, the transmission distance was tested over 100 km SMF (Figure 35 middle), yielding minor performance loss, mostly due to setup imperfections. Upon using both polarizations (POL) yielded SNR degradation of ~1dB (likely due to dual-POL PAPR). In addition we measured the performance as a function of sub-band number (Figure 35 right) and again as expected we see some degradation in performance, mainly due to ADC filter attenuation in all measurements, the tested BER was under the soft FEC 3.8e-3 limit, indicating feasibility for practical optical OS-OFDM implementations at very high spectral and power efficiency.

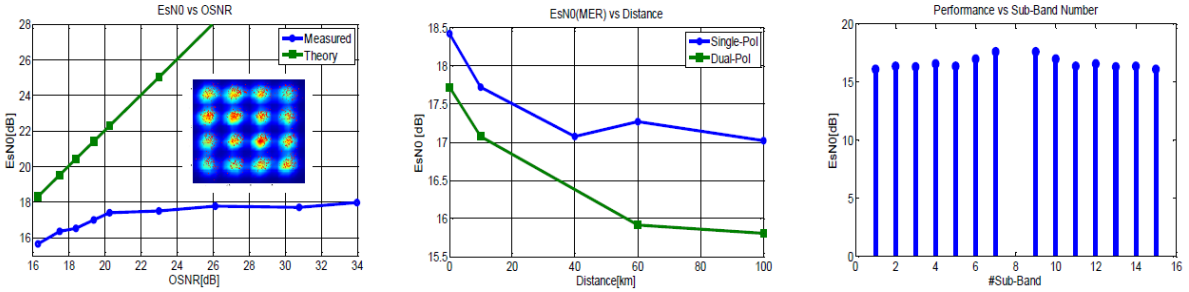


Figure 35: Experimental results: (left) Measured EsN0 (MER) for various OSNR conditions (middle) Measured EsN0 (MER) vs reach (right) Measured EsN0 (MER) per sub-band (bar-chart) over the various sub-bands (degradation away from center due to ADC/DAC.

Achievement: In just 3 FPGAs we realize fastest (180 Gbps) real-time filter-bank based OS-OFDM 16-QAM 25 GHz Rx, at record 1.06 samples/symbol (7.3 b/Hz), demonstrating dual polarization SMF transmission [5].

In ASTRON, the OS-OFDM transceiver can adapt to the channels requirements by partially reconfiguring the implemented FEC module [6]. The dynamic reconfiguration is used in order to load the right version of the ASTRON QC-LDPC FEC code based on the code rate and the block size that is required. The architecture of the proposed scheme is shown in Figure 36.

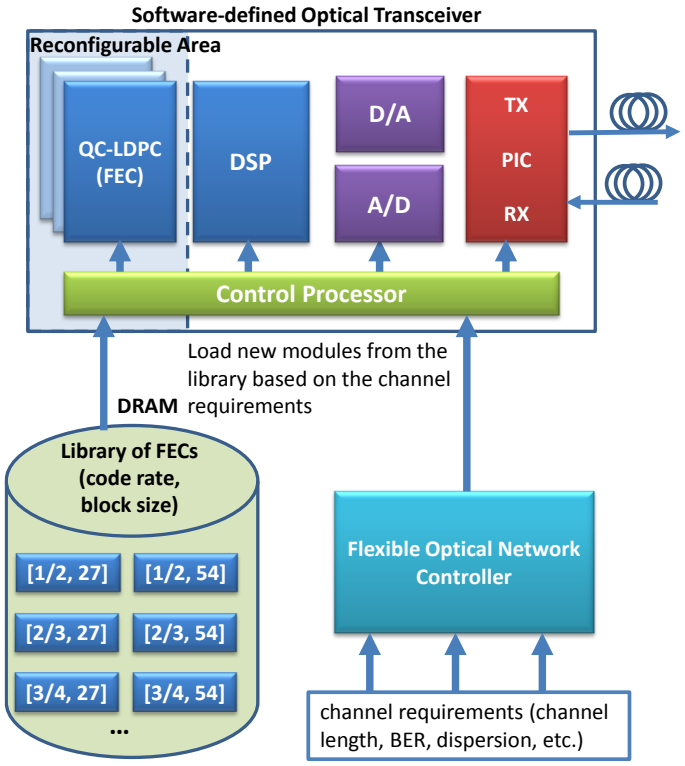


Figure 36. Dynamic reconfigurable LDPC FEC code for flexible optical transceivers.

The software-defined optical transceiver is divided into two parts. The first part contains all the modules that are fixed for this transceiver (optical and electrical frontend), such as the PIC components and the mixed-signal modules (A/D, D/A), whereas the second one is the reconfigurable part that can be configured dynamically without disrupting the operation of the first part and is based on an FPGA. As can be seen, the reconfigurable area contains the signal processing units (DSP modules and the FEC codes required for the error correction of the optical channel). The transceiver also contains the control unit that is used for the control and the reconfiguration of these modules. Outside of the transceiver, there is a storage unit (DRAM or FLASH module) that is used to store the library of the available implemented LDPC FEC codes [7]. The various FEC codes are stored in the memory units as configuration files (bit-streams). Whenever it is required (e.g. due to different application or any change in the optical channel), the Flexible-optical Network Controller (i.e. SDN controller) is used to notify the transceiver that a new FEC code needs to be used. The control processor receives the commands in the optical transceiver from the Optical Network Controller. Then, it loads the corresponding FEC module from the storage unit, and finally, it reconfigures the optical transceiver without disrupting the operation of the rest of the transceiver. When the control processor has finished the reconfiguration of the FEC module, it notifies the optical network controller that the transceiver has been configured. While the configuration takes place, the incoming packets (i.e. for the receivers) are temporarily stored in a buffer. When the reconfiguration is finalized, the receiver can resume the processing of the packets from the buffer using the updated LDPC code for the FEC checking. In general, the control units are used to reconfigure the optical transmitter without disrupting the transmitted data. At the same time, the receiver is reconfigured to the same configuration with the transmitter, in terms of FEC, bit rate and modulation format.

To experimentally demonstrate the capability of the ASTRON transceiver in the AO-OFDM configuration, an experimental testbed was set at NICT's Laboratories, using both direct detection with differential phase shifted keying (DPSK) and differential quadrature phase shifted keying (DQPSK) modulation, and coherent detection with QPSK modulation. 7-user, 12.5 Gbaud/user transmission was successfully demonstrated over 40 km of single mode fiber. Figure 37 shows the experimental TX setup for a 7- user DQPSK-modulated AO-OFDM system; the subcarrier spacing equates the symbol rate B=12.5 GHz, to achieve the

maximum spectral efficiency. Figure 38 shows the optical comb spectrum and time domain pulses. Figure 39 shows the optical spectrum at the wavelength selective switch (WSS) output.

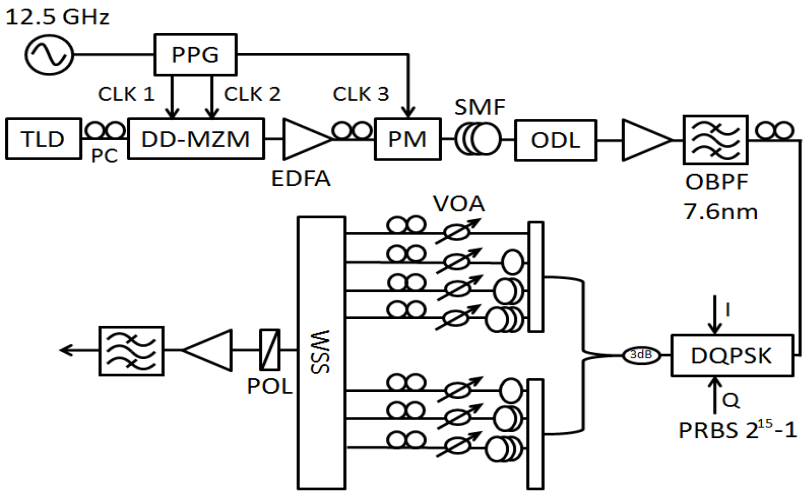


Figure 37: Transmitter setup. Tunable laser diode (TLD), polarization controller (PC), dual-drive Mach-Zehnder (DD-MZM), pulse pattern generator (PPG), erbium-doped fiber amplifier (EDFA), clock (CLK), phase-modulator (PM), single mode fiber (SMF), optical delay line (ODL), optical band pass filter (OBPF), differential quadrature phase shift keying (DQPSK) modulator, variable optical attenuator (VOA), wavelength selective switch (WSS), polarization scrambling (POL), pseudo random bit sequence (PRBS).

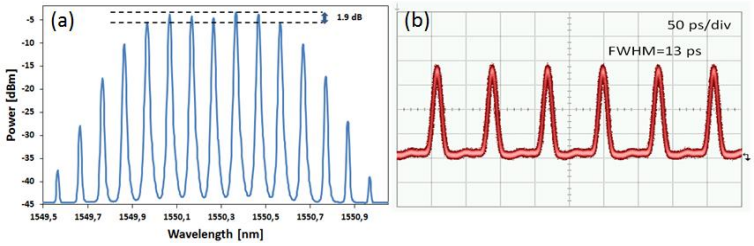


Figure 38: (a) Measured optical comb. (b) Measured Gaussian pulses.

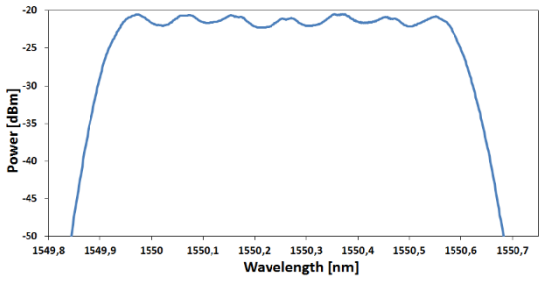


Figure 39: Measured optical spectrum at the WSS output.

Figure 40 shows the RX setup which consists of a VOA and a 20-dB coupler before the AWG in order to measure the received power with a power meter (PWM). The AWG has 16 ports, 200 GHz free spectral range (FSR), 12.5 GHz subcarrier spacing and 10 dB insertion loss. We use a pre-amplifier, a 7.6-nm OBPF, a one-bit delay line interferometer (DLI) and a balanced photo-detector (BPD), with 45 GHz bandwidth, to measure the bit error rate (BER). The BER tester (BERT) supports line rates up to 32 Gb/s.

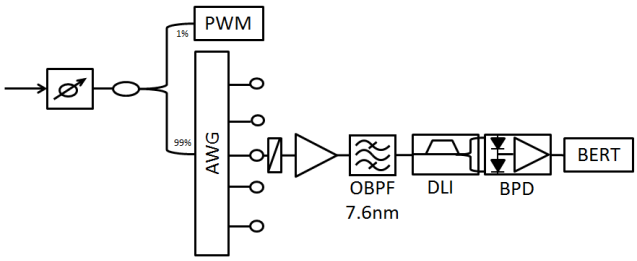


Figure 40: Receiver setup. Power meter (PWM), arrayed waveguide grating (AWG), delay line interferometer (DLI), balanced photodetector (BPD), bit-error rate tester (BERT).

Roma3 and NICT extended the analysis considering also a fiber Bragg grating (FBG) at the RX, to filter the AO-OFDM signal. The use of a FBG is advantageous to reduce the costs in optical access networks. Figure 41 shows the experimental setup for three 12.5 Gb/s DPSK modulated subcarriers. The TX is same as that of setup in Figure 37; at the RX side a FBG is used, with a *sinc*-shaped transfer function to filter a single AO-OFDM subcarrier, with 20 dB insertion loss. A VOA is used to vary the received optical power after the FBG.

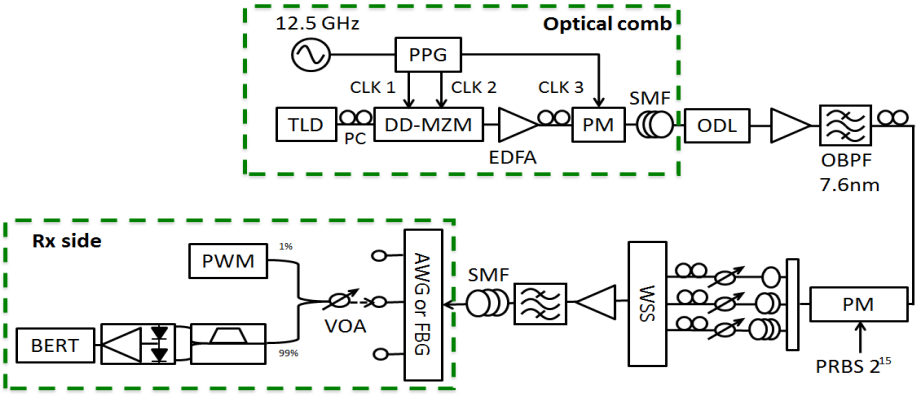


Figure 41: Experimental setup of an AO-OFDM system using either AWG or FBG at the receiver.

The measured eye diagrams of a seven channel B2B system, and after 35-km SMF are reported in Figure 42(a) and Figure 42(b), respectively; no optical time gating or CD compensation have been used. Figure 43(a) reports the received spectrum at an AWG output port, for a transmission of seven AO-OFDM subcarriers, and Figure 43(b) refers to the case when the target subcarrier is not transmitted, i.e. measures the ICI at the same port from the other six carriers. The measured crosstalk is -35.6 dBm. Figure 44 reports the BER measurements as a function of the total received power. The B2B behaviour is compared with the performance obtained with the same setup, using QPSK modulation and coherent detection. In the case of coherent detection, five adjacent subcarriers, spaced 12.5 GHz each, are taken into account. DQPSK-modulated subcarrier in B2B presents about 3-dB penalty at BER=10^{-6} with respect to coherent detection.

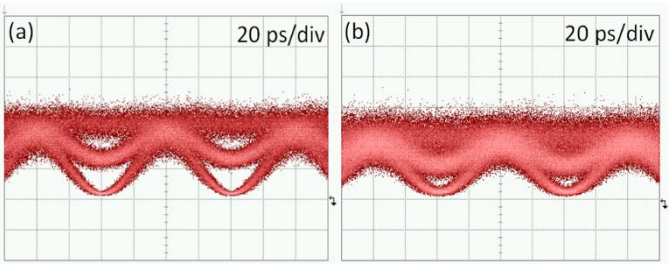


Figure 42: Measured eye diagrams of a 7 channel transmission (a) B2B (b) after 35-km SMF.

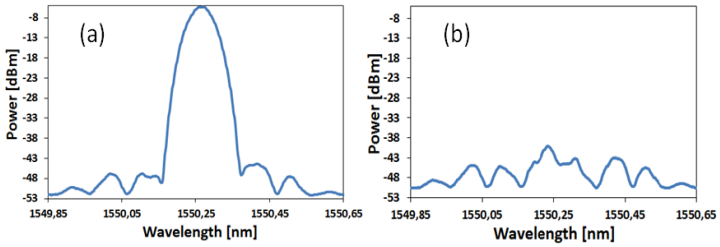


Figure 43: Spectrum measured at an AWG output port (a) transmitting seven AO-OFDM carriers (b) transmitting six subcarriers (the target subcarrier has been switched off).

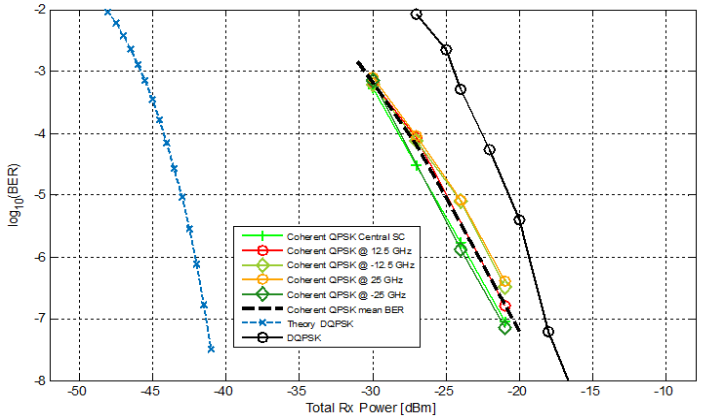


Figure 44: BER vs received power in BTB for a DQPSK-modulated subcarrier received with direct detection compared with five QPSK subcarriers received by coherent detection (the dashed line corresponds to the mean BER curve of the five subcarriers). A theoretical curve for direct detection is also shown for reference.

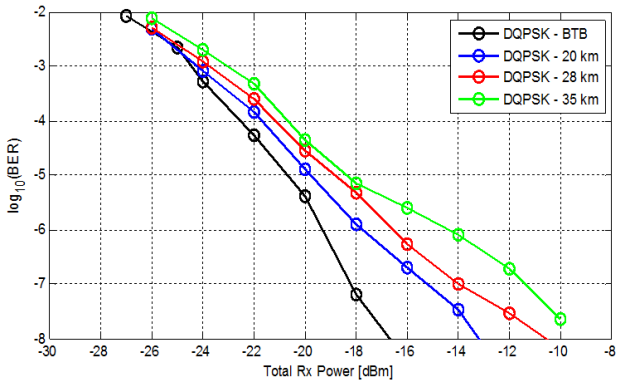


Figure 45: BER vs received power for a DQPSK-modulated subcarrier for B2B, 20-km, 28-km, and 35-km transmission over uncompensated SMF.

Figure 45 reports BER measurements after 20 km, 28 km and 35 km SMF for single DQSPK modulated subcarrier, without any dispersion compensation. Error-free transmission is achieved for all the subcarriers.

Conclusion and Expected Impact

ASTRON Project, in spite of the difficulties encountered on some aspects of the platform integration, has opened several paths for exploitation:

- At the component level, arrays of modulators, photodiodes and planar waveguide based devices were fabricated targeting novel specifications that advancing significantly the state of the art towards Tbps applications.

- On the DSP and FEC sides, the ASTRON project delivered a set of competitive solutions that maintain good performance, but also offer reduced implementation complexity and power consumption.

Partners have gained significant knowledge on how to design and fabricate such devices and on how to improve their processes.

Even if a full integrated Terabit transceiver platform was not completed at the end of the project, this is not a show stopper since the introduction of Tbps transceivers is expected by 2019-2020 time-scale, which is a time-target that the ASTRON partner can meet. In addition the ASTRON technology can be used in alternative implementations, where PICs operating at lower rate are used as pluggable units of a Terabit card (see IDEALIST BV-Transceiver architecture).

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Acronyms List

A/D	Analog-to-Digital
D/A	Digital-to-Analog
ADC	Analog-to-Digital Converter
AO-OFDM	All-optical OFDM
ASIC	Application-Specific Integrated Circuit
AWG	Arrayed Waveguide Grating
BER	Bit Error Rate
BERT	BER tester
CAD	Computer-Aided Design
CD	Chromatic Dispersion
CLK	Clock
CMOS	Complementary Metal-Oxide Semiconductor
CPW	Coplanar Waveguide
CPS	Coplanar Strip
DAC	Digital-to-Analog Converter
DBP-SSF	Digital Back-Propagation Based On Split-Step Fourier Method
DC	Direct Current
DD-MZM	Dual-Drive Mach-Zehnder
DFT	Discrete Fourier Transform
DQPSK	Differential Quadrature Phase Shift Keying
DSP	Digital Signal Processor
dual-POL	*Dual-polarized*
PAPR	Peak To Average Power Ratio
EDFA	Erbium-Doped Fiber Amplifier
ENOB	Effective Number of bits
EVM	Error Vector Magnitude
FBG	Fiber Bragg Grating
FEC	Forward Error Correction
FPGA	Field-Programmable Gate Array
FSR	Free Spectral Range
HSR	High Spectral Resolution
ICRF	Integration Cost Reduction Factor
IDFT	Inverse Discrete Fourier Transform
InP	Indium phosphide
IVSFT-NLE	Inverse Volterra Series Transfer Function Nonlinear Equalizer
QC-LDPC	Quasi-Cyclic LDPC
LDPC	Low-Density Parity-Check
LPF BW	Low Pass Filter Bandwidth
MER	Modulation Error Ratio
MMI	Multi-Mode Interference
MZ	Mach-Zehnder
MZM	Mach-Zehnder Modulator
IQ	In Phase quadrature
NFDM	Nyquist Frequency Division Multiplex

OBPF	Optical Band Pass Filter
ODL	Optical Delay Line
OFDM	Orthogonal Frequency-Division Multiplexing
OSNR	Optical To Signal To Noise Ratio
OS-OFDM	Optically-shaped OFDM
OTU	Optical Transport Unit
PC	Polarization Controller
PCB	Planar Connection Boards
PD	Photo-Detector
PIC	Photonic Integrated Circuit
PLC	Planar Lightwave Circuit
PM	Phase-Modulator
POG	PIC-on-Glass
POL	Polarization Scrambling
PON	Passive Optical Network
PPG	Pulse Pattern Generator
PRBS	Pseudo Random bit Sequence
PTG	PIC-to-Glass
PWM	Power meter
QAM	Quadrature Amplitude Modulation
QC-LDPC	Quasi-Cyclic Low Density Parity Check
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
Rx	Receiver
SDN	Software Defined Network
SLICE	Selective Laser Induced Chemical Etching
SMF	Single Mode Fiber
TEC	Thermal Electric Cooler
TLD	Tuneable laser diode
TWE	Travelling Wave Electrode
Tx	Transmitter
VOA	Variable Optical Attenuator
WDM	Wavelength-Division Multiplexing
WSS	wavelength selective switch
XT	Cross-Talk